Preliminary

IOP Board

Schematics

Rev : A
Date : 06/07/84

By : A. K. Tsang
R. Knauss
J. Oloumi
R. Swenson
G. Thompson

File : [Ibis]<Daisy>IOP>DesignReview>Schematics.press

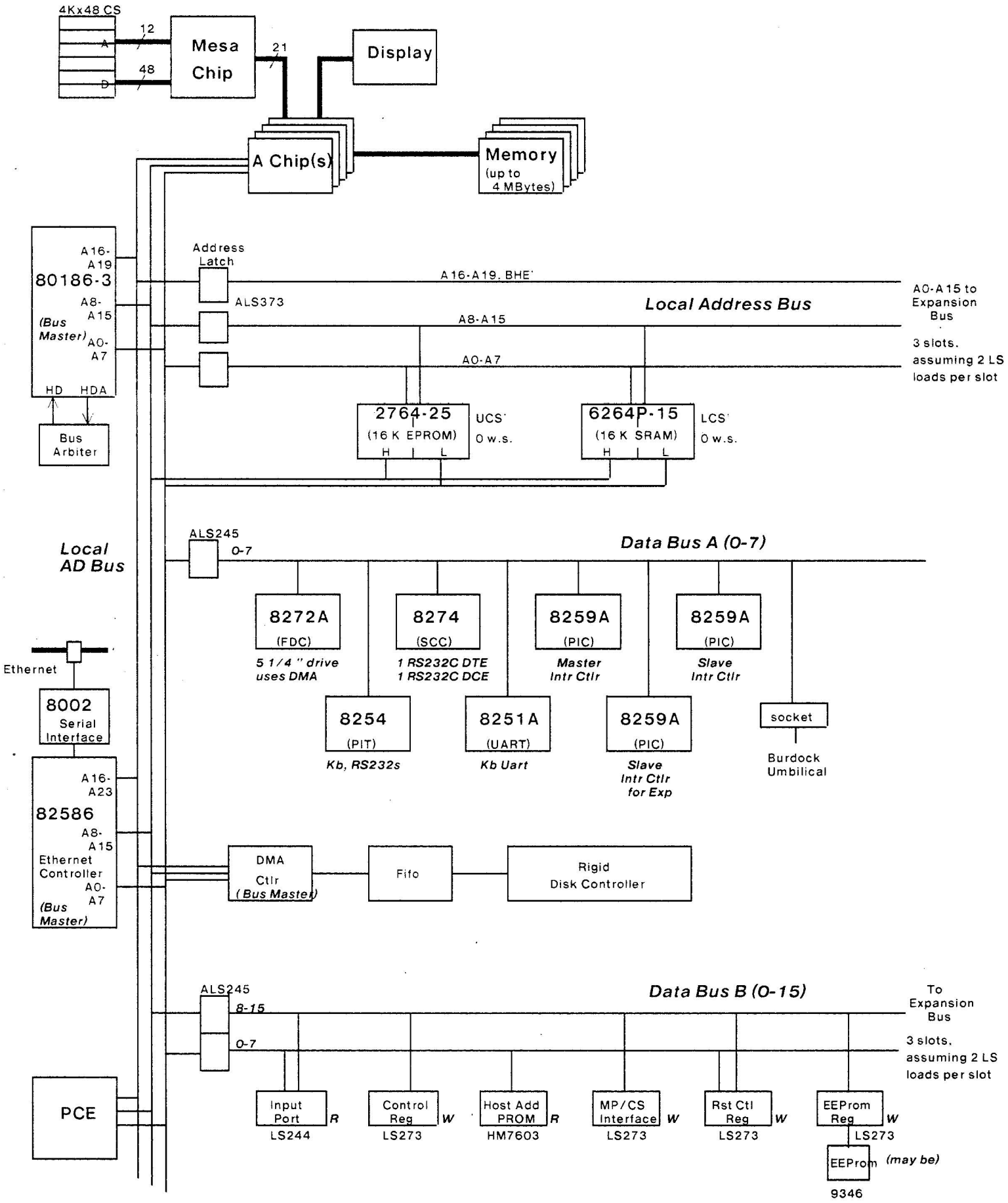
XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dove	IOP Schematics	IOP0.silx	Tsang	A	6/06/84	0

Logic Drawings

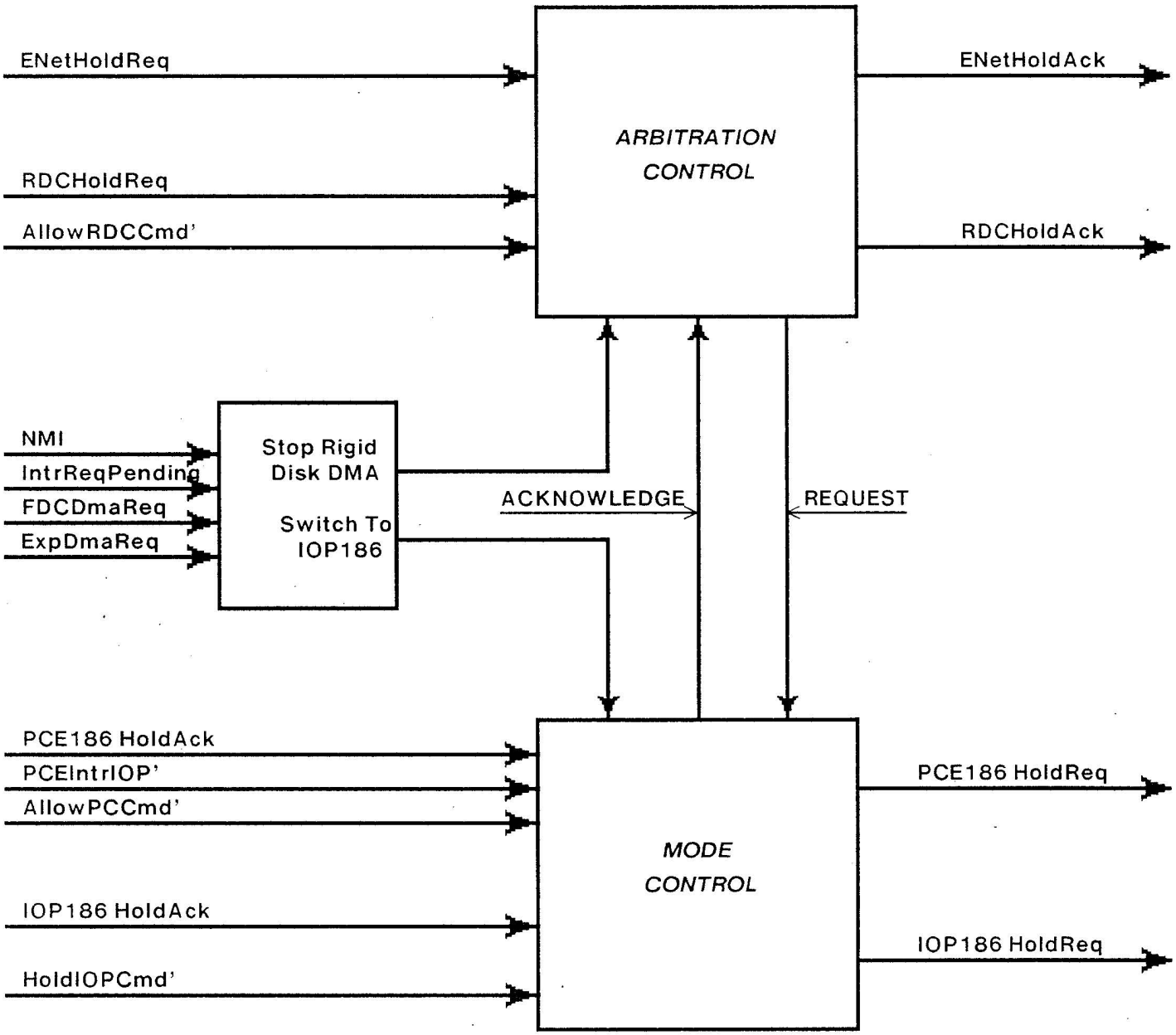
Others for SW boards :

A-Chip Interface Logic
Mid-Ram & LED Display
MultiBus Chassis Connector
Dip-Switch
KB RS232 D/R & DIP Socket
Connection for Hold-LEDs
Signals for Arbitor States
RDC LED Display
Platforms

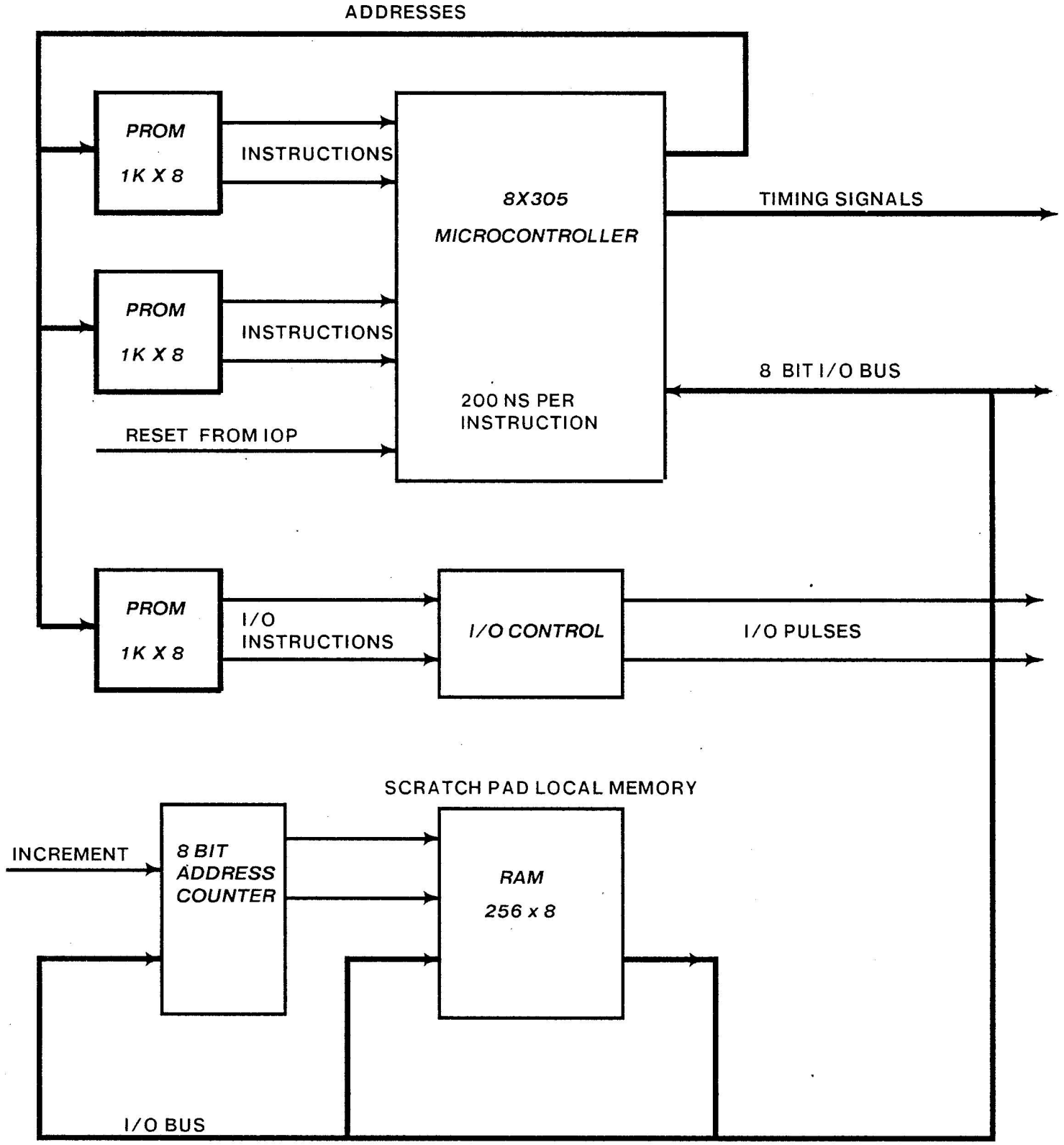
XEROX SDD	Project	Table of Contents -- Logic Drawings	File	Designer	Rev	Date	Page
	Dove		IOP00.silx	Tsang	A	6/06/84	00



XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dove	IOP Block Diagram	IOP61.silx	Tsang	A	6/1/84	61

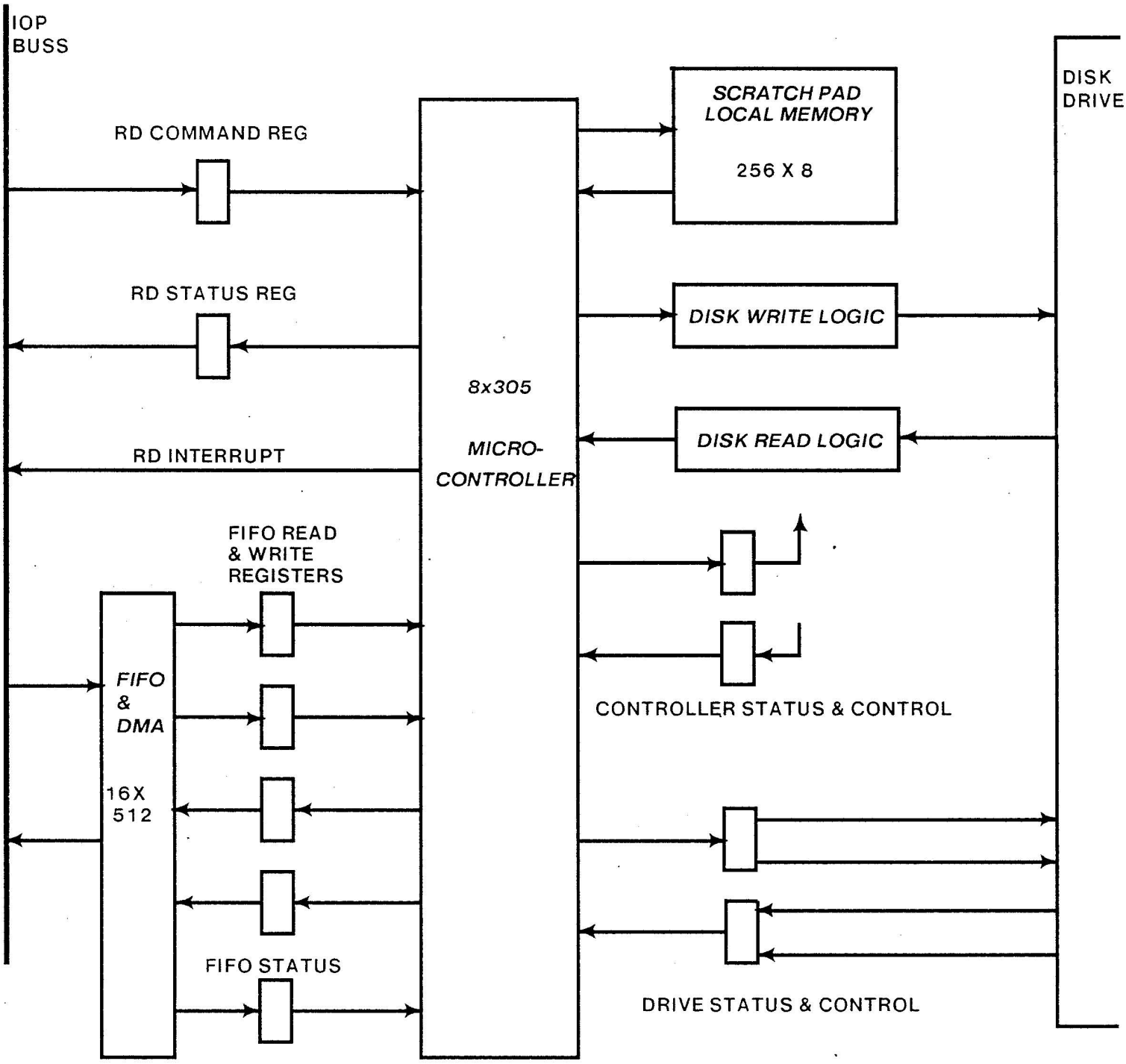


XEROX SDD	Project: Dove	Arbitor Block Diagram	File: IOP62.silx	Designer: Knauss	Rev: A	Date: 6/06/84	Page: 62



XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dove	8x305 MicroController	IOP65.silx	Swenson	A	6/06/84	65

RIGID DISK CONTROLLER
BLOCK DIAGRAM



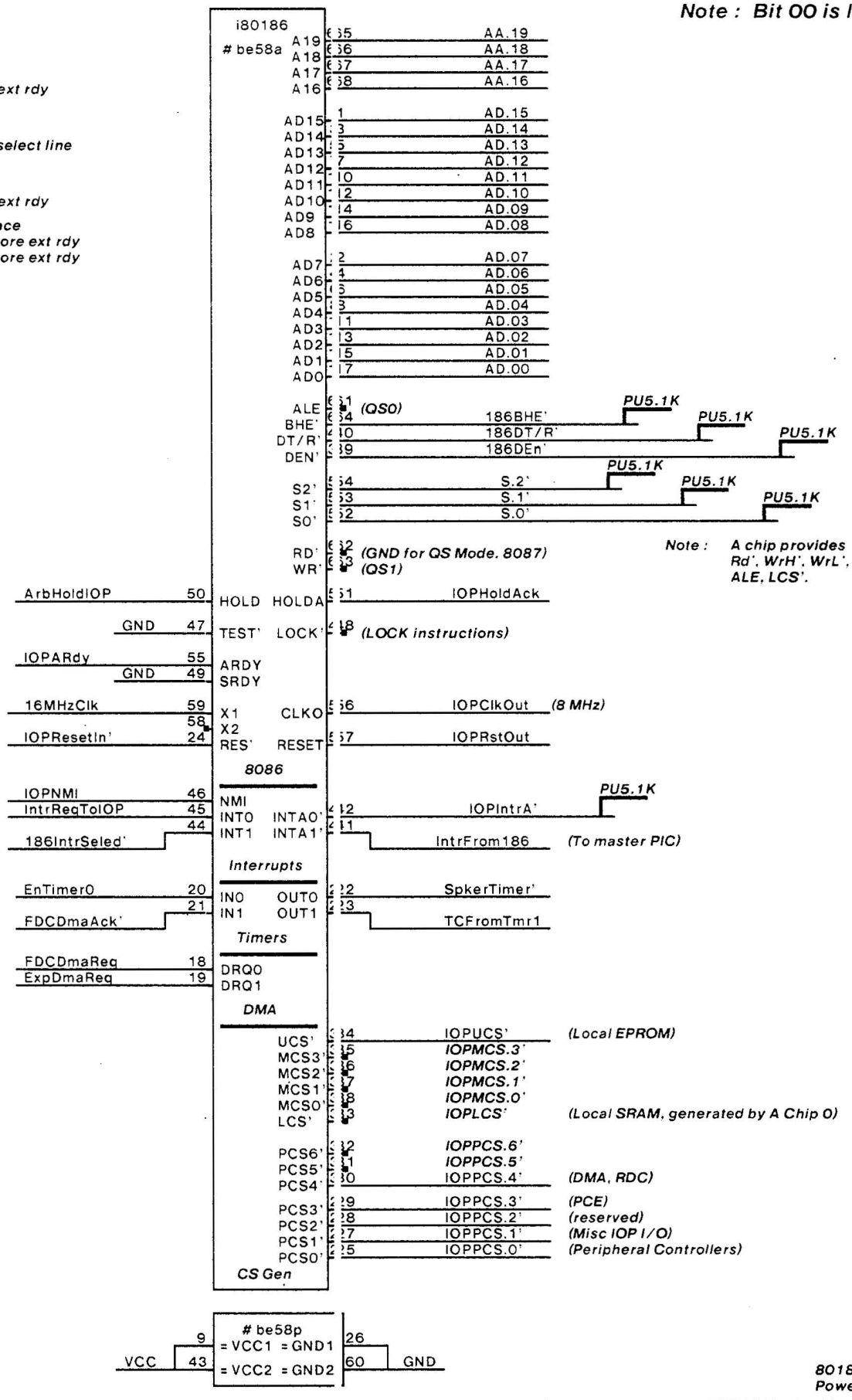
XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dove	RDC Block Diagram	IOP66.silx	Swenson	A	6/06/84	66

IOP

Note : Bit 00 is lsb

Programming Notes :

1. *UCS : EPROM*
   16 KBytes. 0 ws, ignore ext rdy
2. *MCS : SRAM*
   base addr = 10000H
   mem size = 16 KBytes/select line
   0 ws, ignore ext rdy
3. *LCS : SRAM*
   16 KBytes. 0 ws, ignore ext rdy
4. *PCS : base addr = 0 in I/O space*
   PCS.0.1.2.3 1 w.s., ignore ext rdy
   PCS.4.5.6 0 w.s., ignore ext rdy



80186 - 0
Power - 1

XEROX SDD	Project Dove	80186 IOP	File pIOP01.sil	Designer Tsang	Rev A	Date 6/04/84	Page 01

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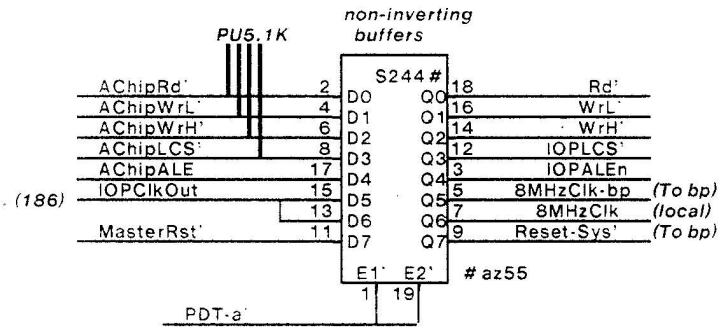
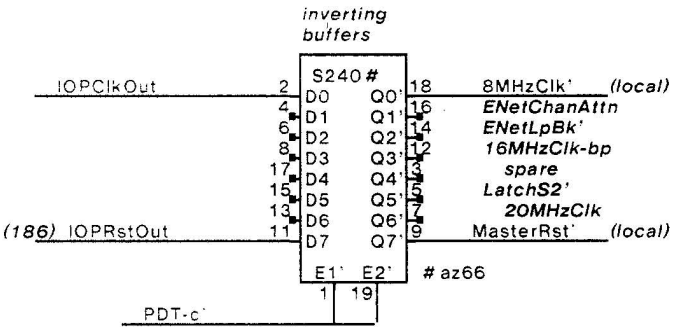
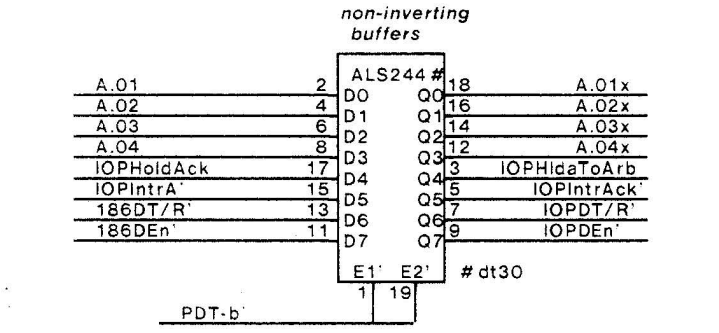
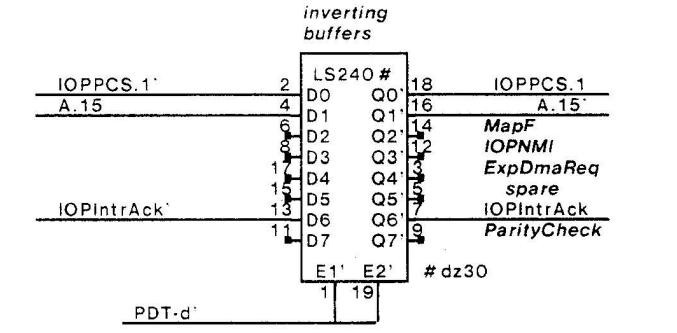
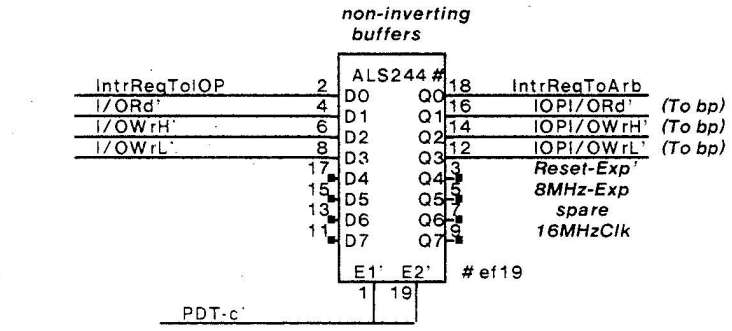
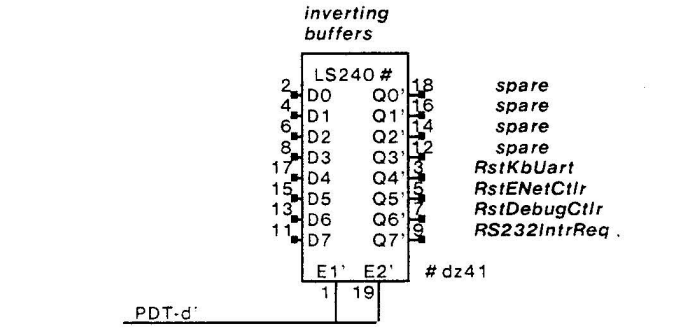


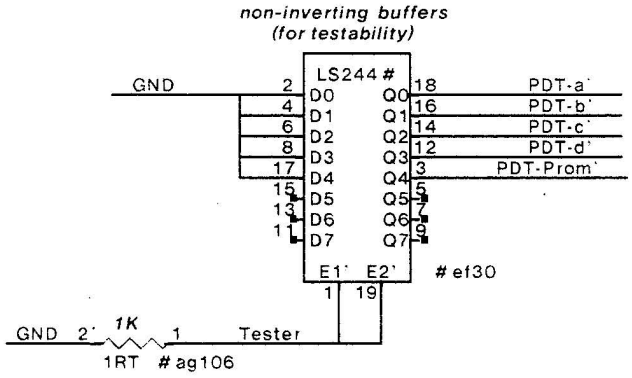


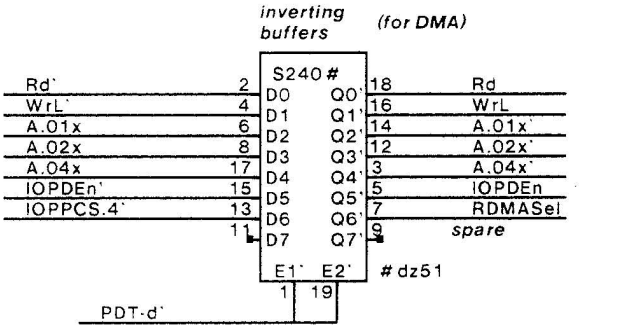












S241, tPD = 6, 9
LS244, tPD = 12, 18
ALS244, tPD = 3, 10

S240, tPD = 5, 7
LS240, tPD = 12, 18
ALS240, tPD = 2, 9

Loadings :

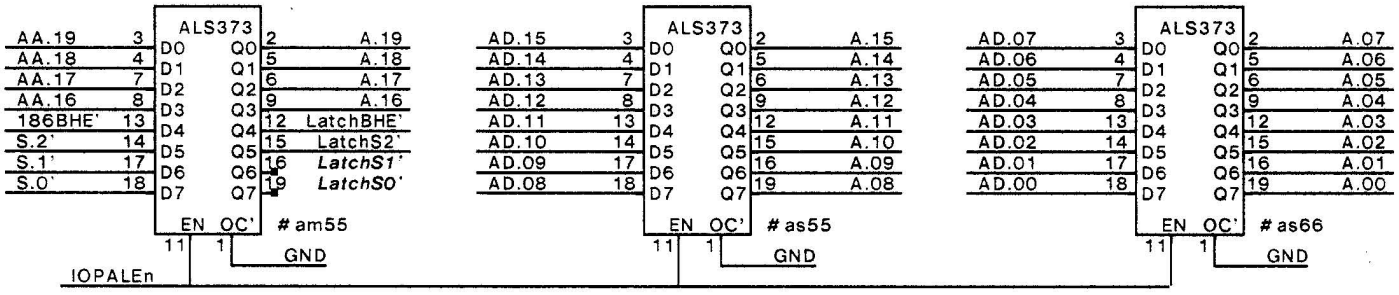
Rd'	12 MOS, 2 LS
WrL'	10 MOS, 2 LS
MasterRst'	10 LS, 1 S

74244 - 2
74240 - 1
Resistor - 0

XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dove	Control Signal Buffering	pIOP02.sil	Tsang	A	6/06/84	02

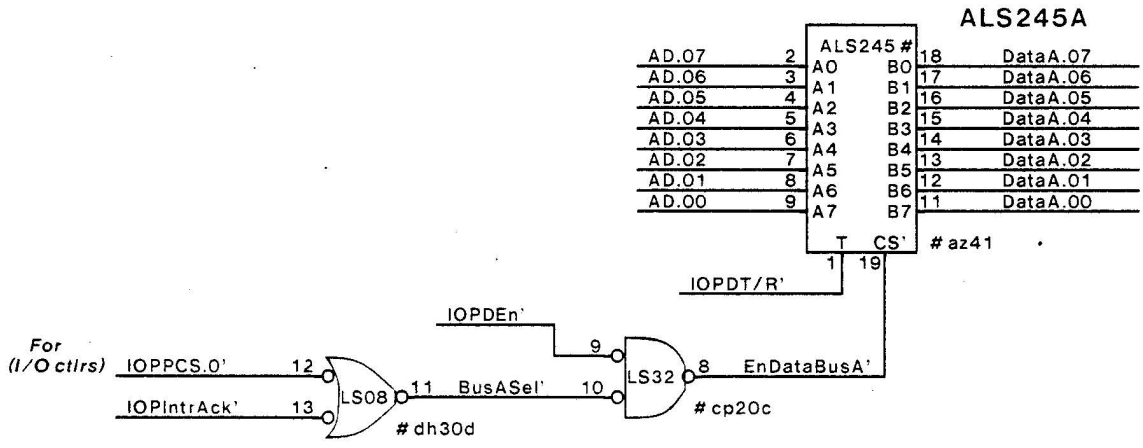
Note: Bit 00 is lsb

Address Bus

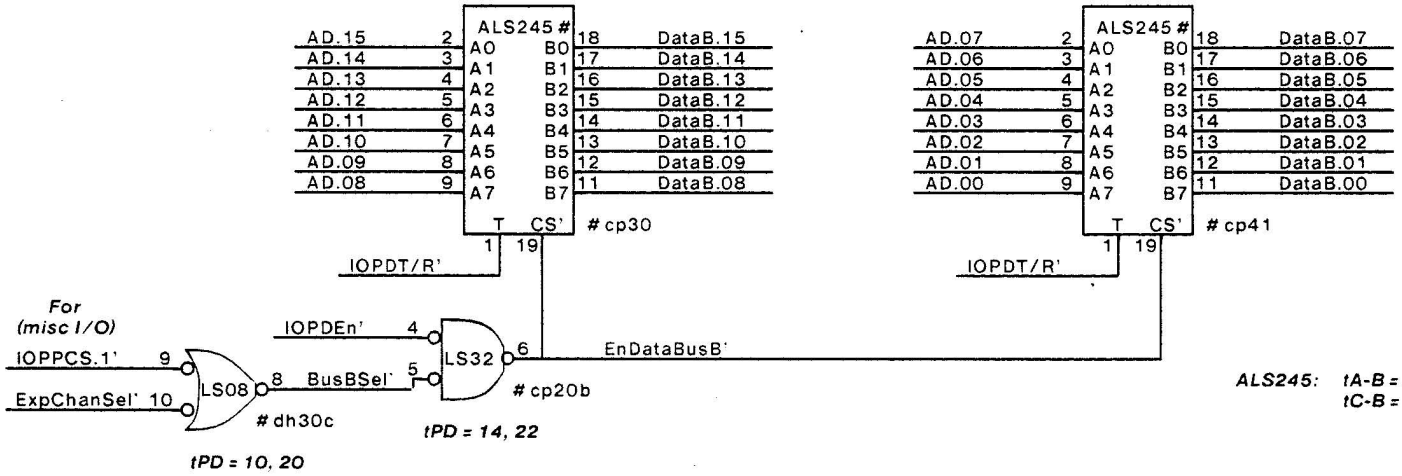


ALS373: tD-Q = 4,16 tE-Q = 6,20
tSU = 10, tH = 7, tW = 10 min

Data Bus A *(8 bit bus)*



Data Bus B *(16 bit bus)*



tPD = 10, 20
tPD = 14, 22

ALS245: tA-B = 3, 10
tC-B = 5, 20

74245 - 0
74373 - 1

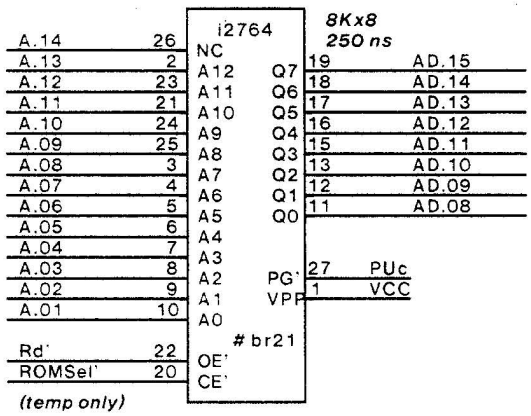
XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dove	Address Latch & Data Buffers	pIOP03.sil	Tsang	A	6/06/84	03

Note : Bit 00 is lsb

16 KBytes of EPROM

(Memory Address : FC000H -- FFFFFH)

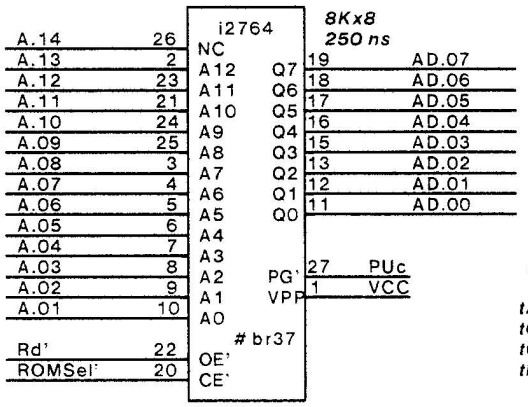
High Byte



(temp only)

Use IOPUCS' for 2nd etch.

Low Byte



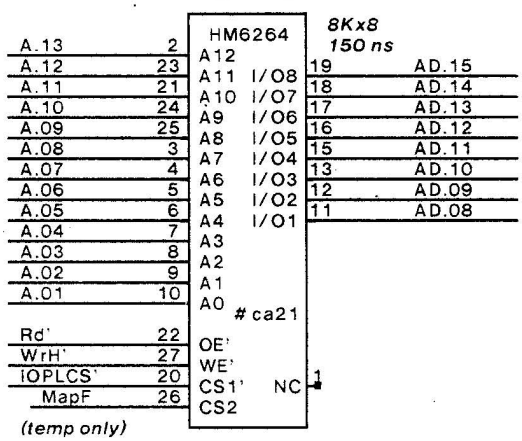
(0 w.s.)

tAA = 250
tCE = 250
tOE = 100
tDF = 60

16 KBytes of SRAM

(Memory Address : 0 -- 3FFFFH)

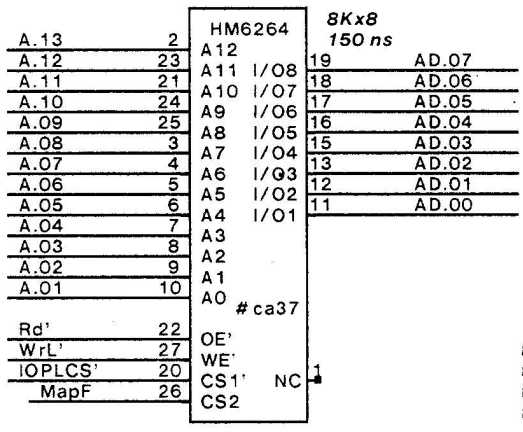
High Byte



(temp only)

Use PUc for 2nd etch

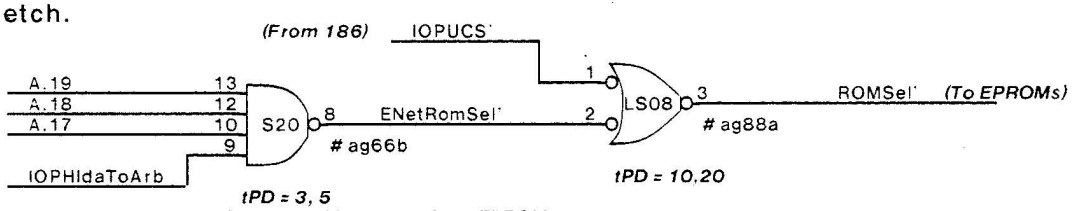
Low Byte



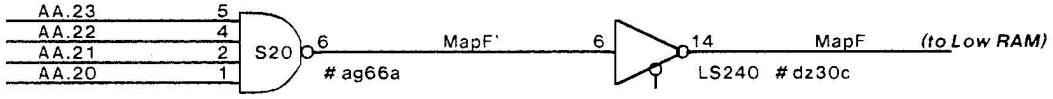
(0 w.s.)

tAA = 150
tCS = 150
tOE = 70
tDF = 50

This section can be removed at 2nd etch.



Note: This circuit is to allow Ethernet chip to boot from EPROM. May be removed when A-Chip memory arrives.



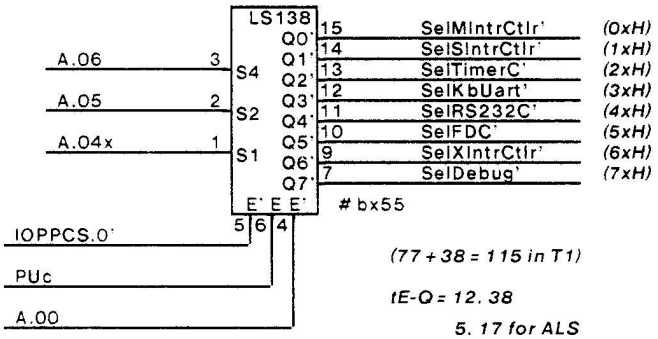
* *Pin 26 of i2764 is connected to A.14 to allow i27128.*

6264 - 2
2764 - 0
2186 - 1

XEROX SDD	Project Dove	Local Memory	File pIOP04.sil	Designer Tsang	Rev A	Date 6/04/84	Page 04

I/O Address Decoding

(All are for 8-bit I/O devices on Data Bus A)



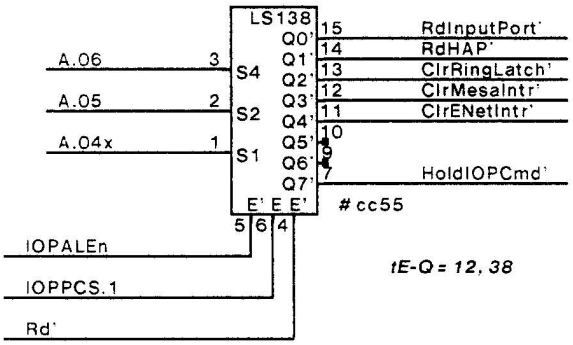
(77 + 38 = 115 in T1)

tE-Q = 12, 38

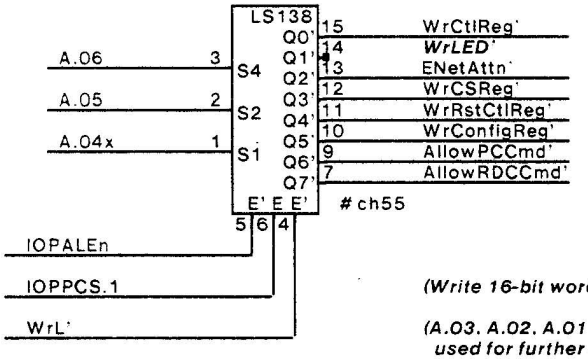
5, 17 for ALS

A.01, A.02, A.03 are used for I/O controllers' address lines.

(All are for 16-bit I/O devices on Data Bus B)



tE-Q = 12, 38



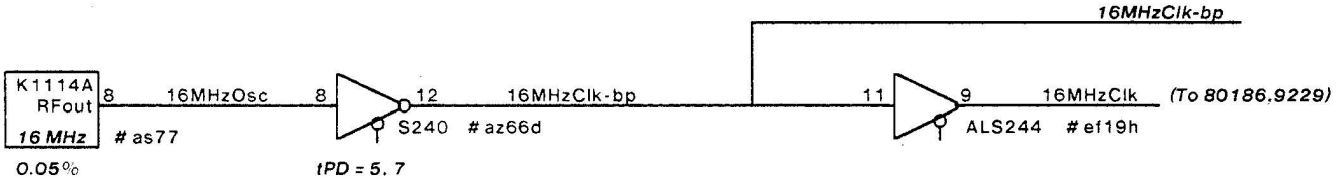
??

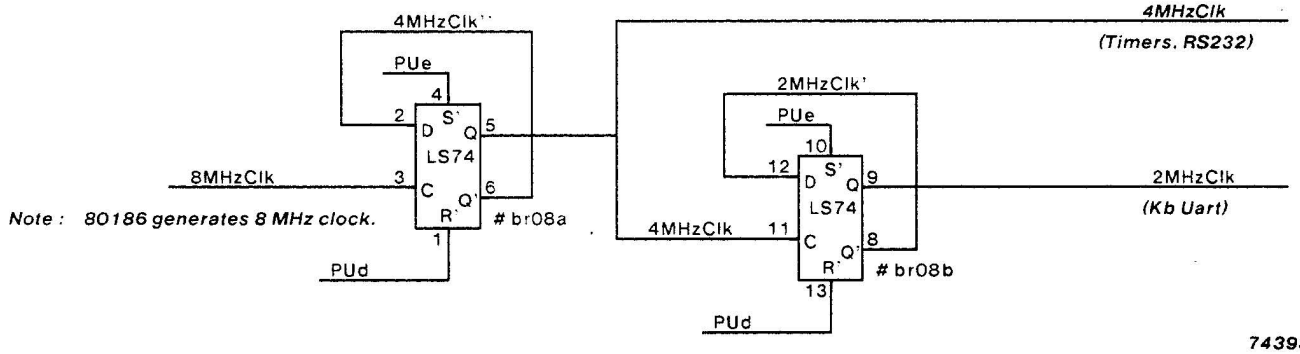
(Write 16-bit words only)

(A.03, A.02, A.01 can be used for further selects)

Clocks

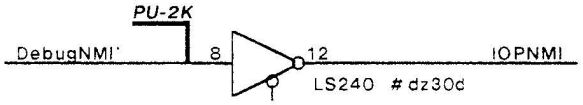
(Terminating R's on bp)



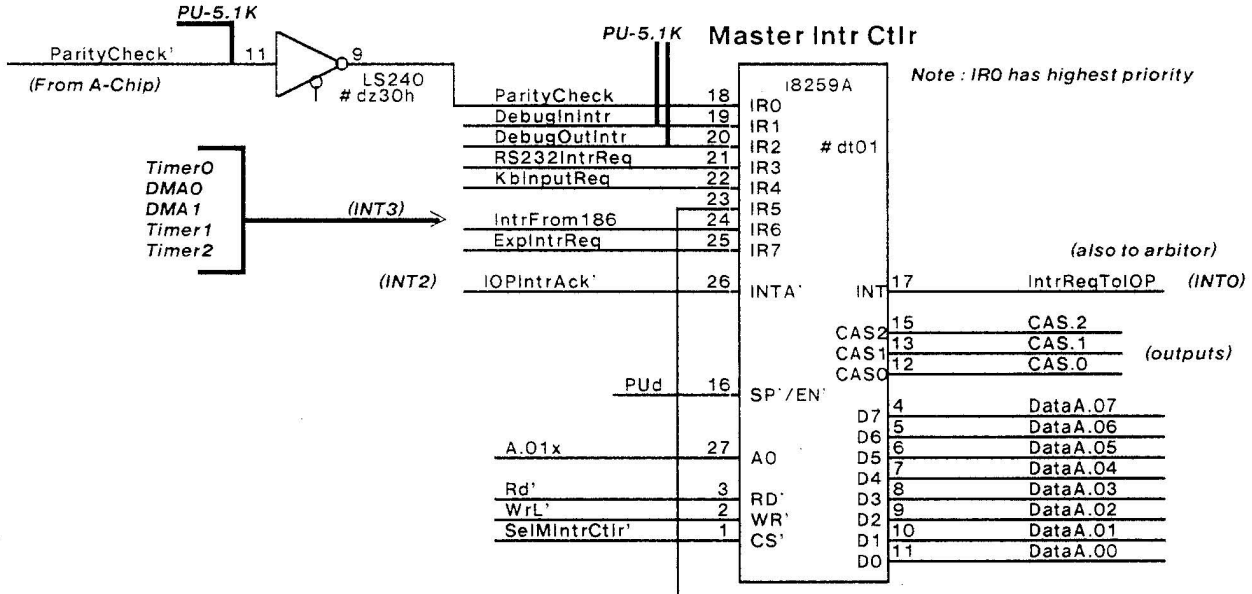


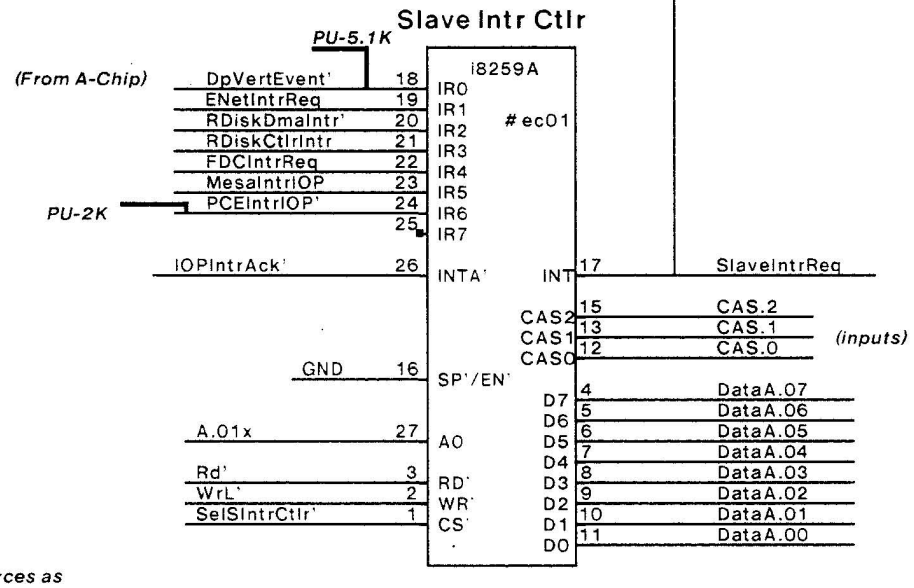
74393 - 1
Resistor - 0

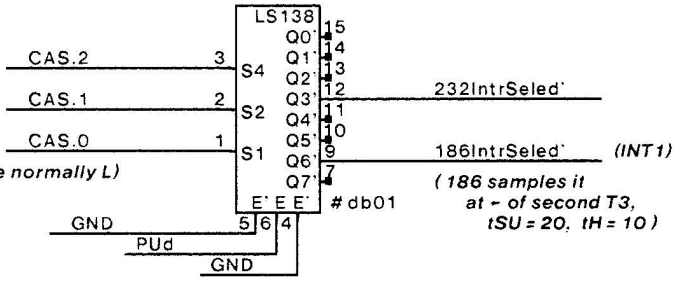
XEROX SDD	Project Dove	I/O Address Decoding & Clocks	File pIOP05.sil	Designer Tsang	Rev A	Date 6/06/84	Page 05



* NMI is an edge-triggered input by a L to H transition and syn. internally.
A duration of one or more c.c. will guarantee service at next inst boundary.







Note:

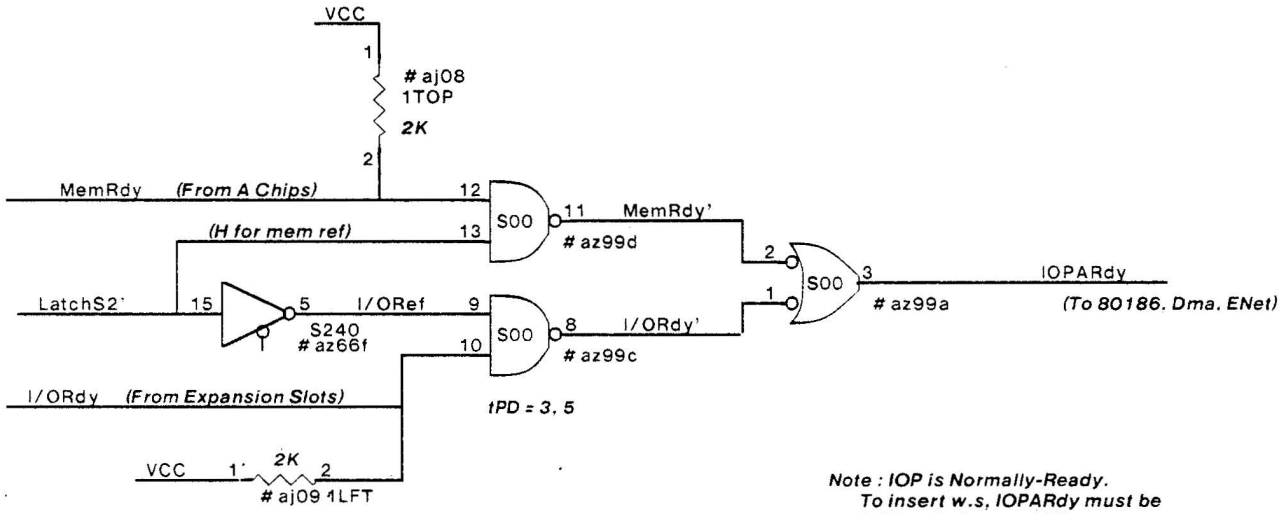
1. 80186 operates in
   * iRMX mode
   * Internal interrupt sources as slaves to ext master PIC
   * Internal vectoring
2. Master PIC operates in
   * as master PIC (ie. SP' = H)
   * non-buffered mode
   * cascade mode
   * special fully nested mode
   * all inputs are edge-triggered
   * slave intr ctlr inputs at : IR3, IR5, IR6, IR7
3. Slave PIC operates in
   * as slave PIC (ie. SP' = L)
   * non-buffered mode
   * cascade mode
   * all inputs are edge-triggered

Resistor - 1
8259 - 0

XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dove	Interrupt Controllers & NMI	pIOP06.sil	Tsang	A	6/06/84	06

Ready Logic

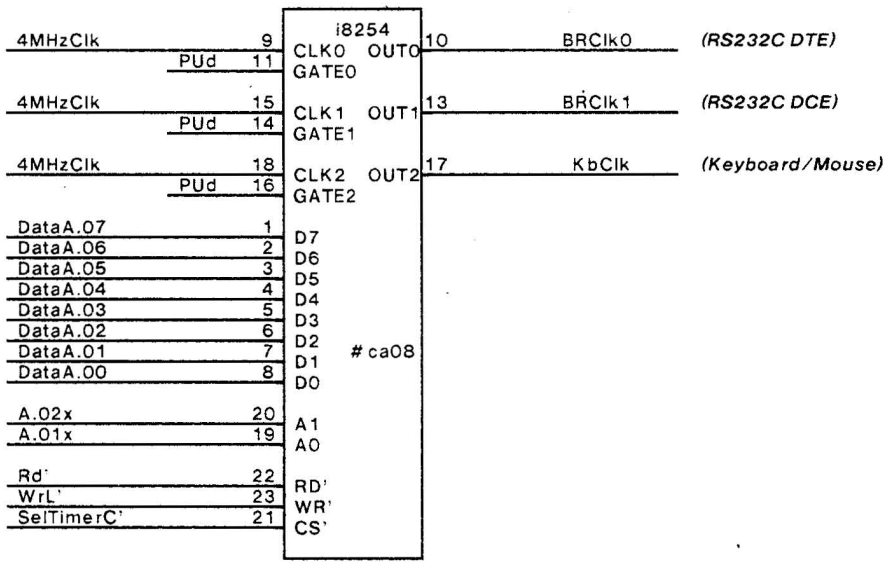
#az99b is used for Expansion Interface



Note : IOP is Normally-Ready. To insert w.s, IOPARdy must be L 35 ns before ↑ of T3.

For Intr Ack cycles, S.2' = L, and so IOPARdy = H. No w.s. is needed because IntrAck' signals become active in T1, early enough to satisfy the access time of 8259A.

Timers

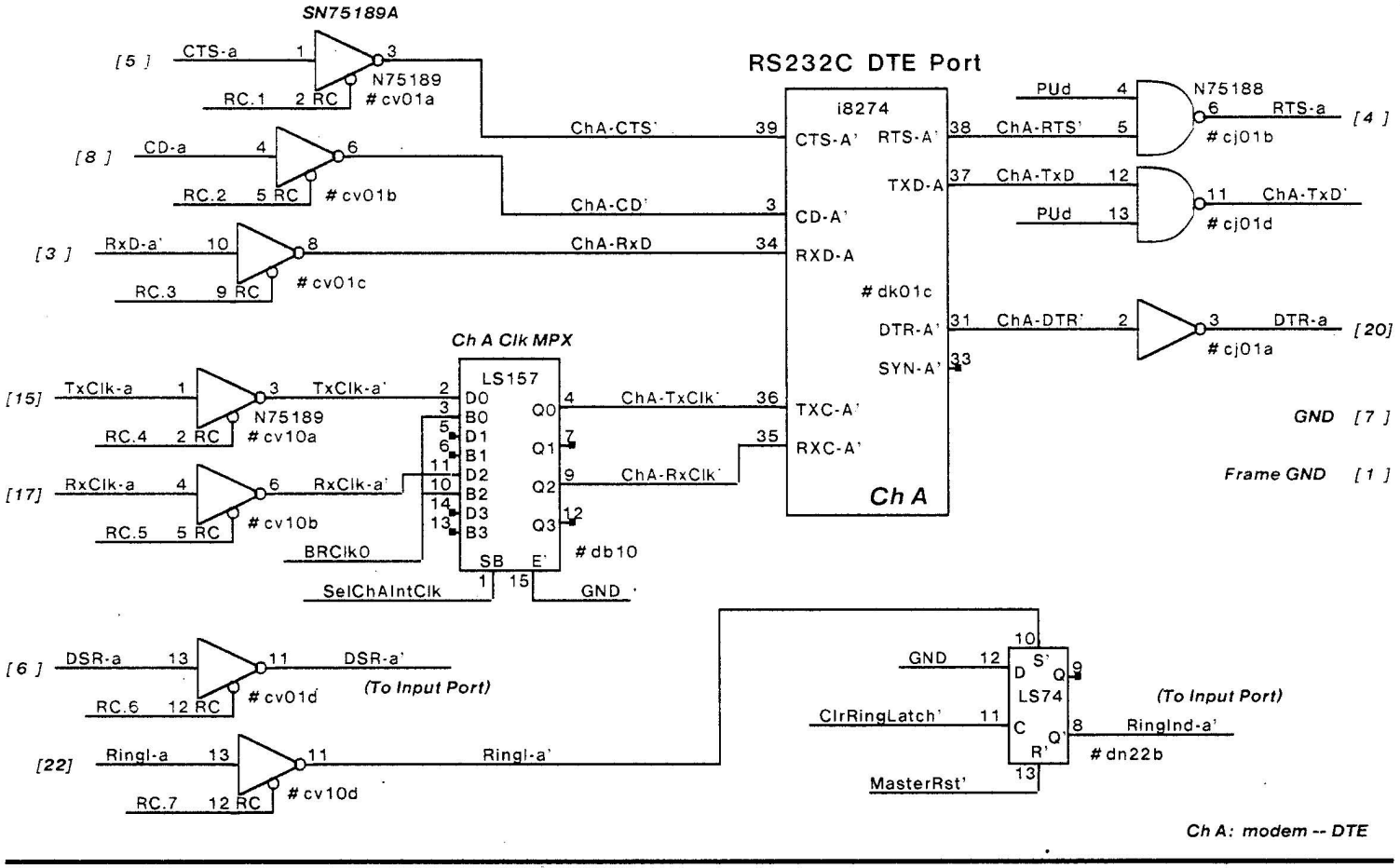


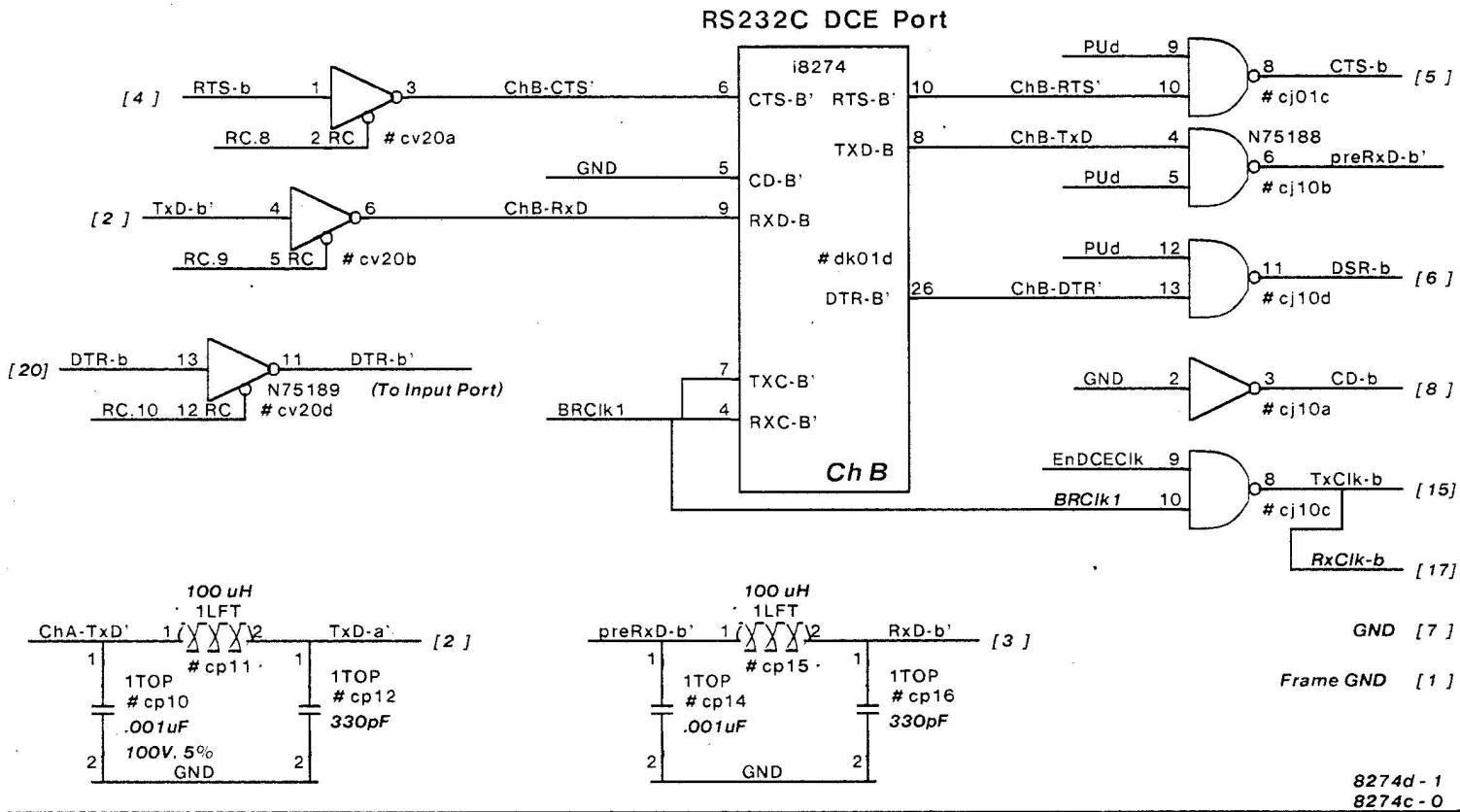
(max clock input freq is 8MHz)

tAR = 45, tAW = 0

8254 - 1

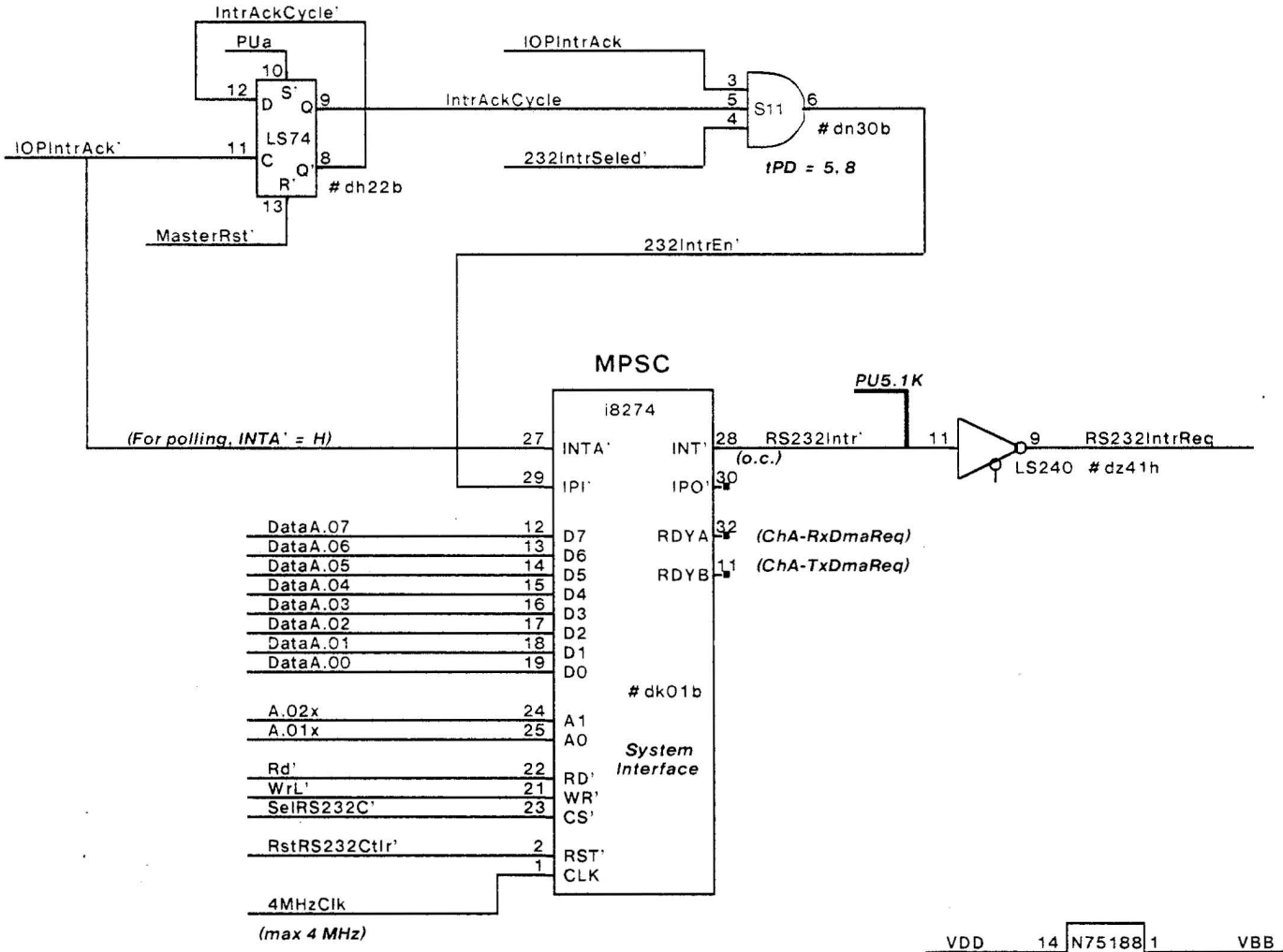
XEROX SDD	Project Dove	Ready Logic & Timers	File pIOP07.sil	Designer Tsang	Rev A	Date 6/06/84	Page 07

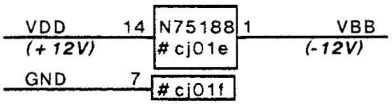


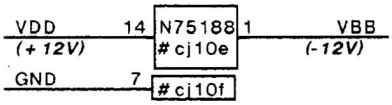


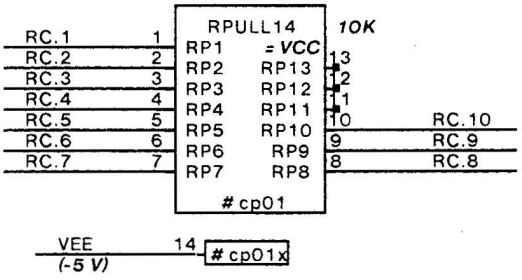
8274d - 1
8274c - 0

XEROX SDD	Project Dove	RS232C DTE & DCE Ports	File pIOP08.sil	Designer Tsang	Rev A	Date 6/06/84	Page 08





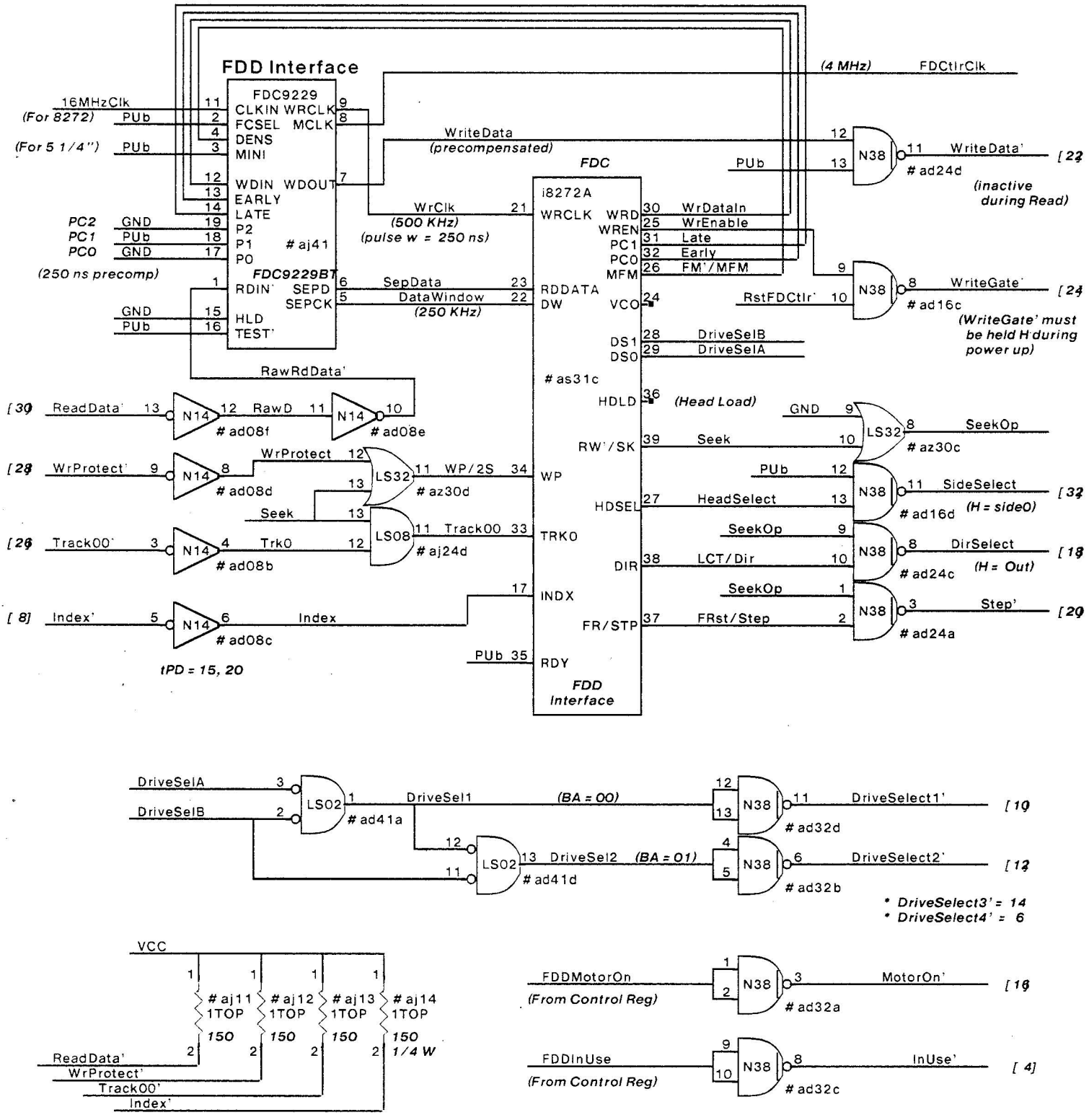




- *8274 operates in interrupt driven mode & vector mode.*
- *Reset must be true for one complete cc for proper int reset (250 ns).*
- *Wr' signal must be > 250ns.*
- *Need 1 w.s. to satisfy tRR, tWW, & tRD.*
- *Leading edge of RD" sets the In-Service Latch.*
- *CPU should read RR2 of Ch.B to determine which internal source requested service (in non-vector mode)*
- *Before leaving intr service routine. must do a EOI to 8274 to reset highest priority source under service.*
- *About IPI'*
  1. *For non-INTA cycle, IntrAckCycle = L, so IPI' is normally L = => allow 8274 to gen intr.*
  2. *During INTA cycle, if IOP is not servicing this 8274, 232IntrSeled' remains H, causing IPI' to be H during second INTA pulse. This will abort the 8274 INTA sequence and prevent it to deliver the interrupt type.*
  3. *During INTA cycle, if IOP is servicing this 8274, 232IntrSeled' will become L during the first INTA pulse and remain L for the rest of the INTA cycle. So IPI' will remain L and 8274 will issue the interrupt type to the bus.*

Resistor - 1
8274b - 0

XEROX SDD	Project: Dove	RS232C Controller System Interface	File: pIOP09.sil	Designer: Tsang	Rev: A	Date: 6/04/84	Page: 09

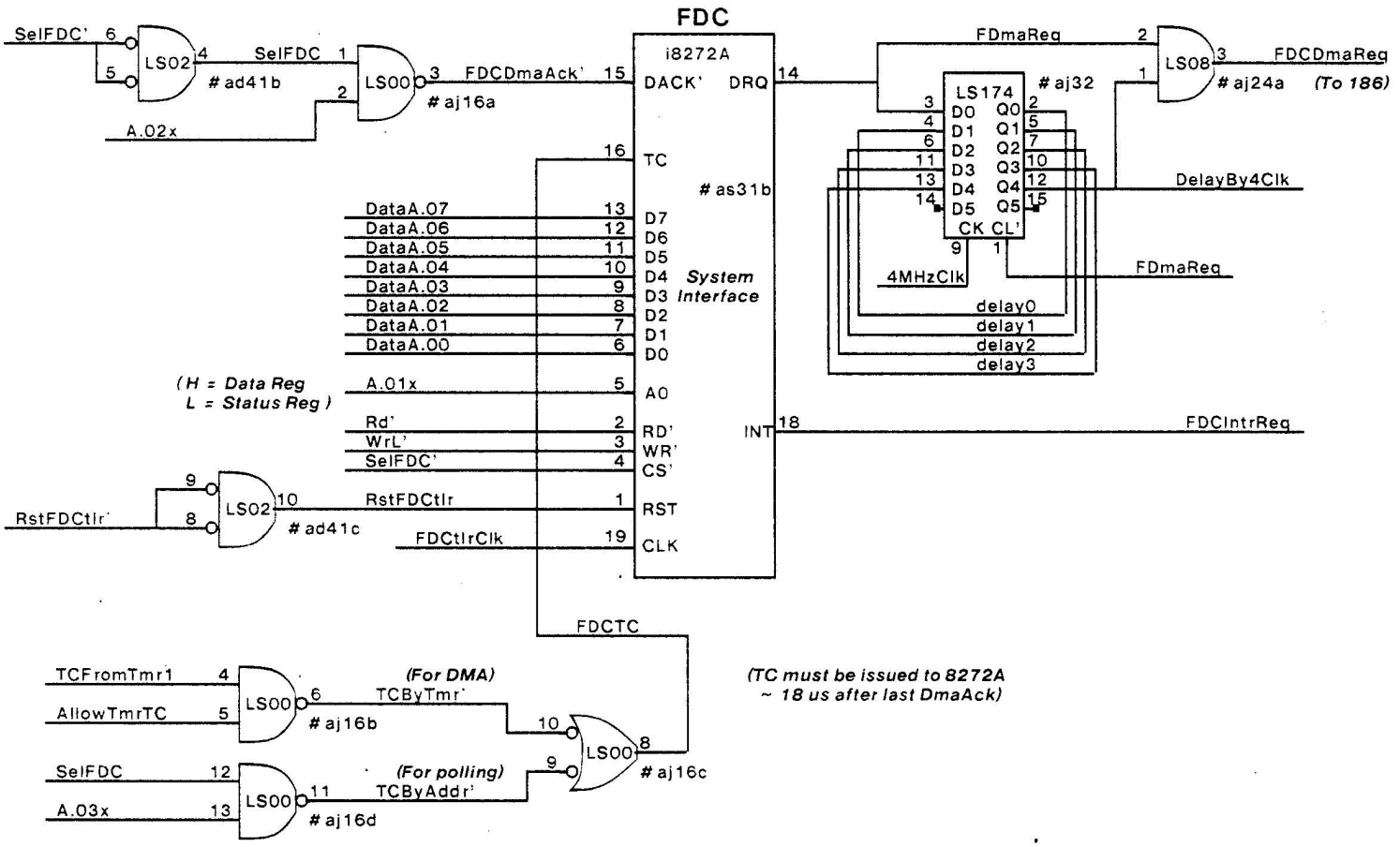


* Not all drive mfgers implement the InUse' signal.
* MotorOn' will turn all motors ON.
A 500 ms delay must be allowed before reading or writing.
For max motor life, deactivate this line if no command has been issued to the drives w/i 2 sec. after completion of a previous command.
* Drive Select signal(s) gate multiplexed input & output lines in drive.

* Support 2 drives only.

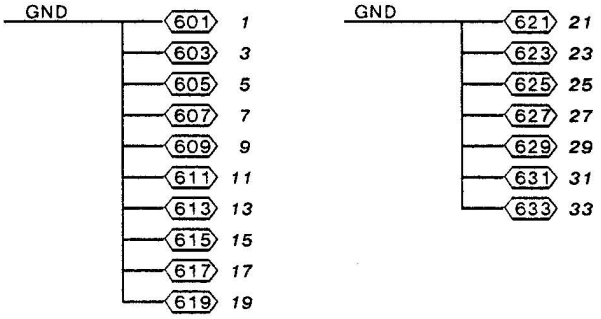
9229 - 1
8272c - 0

XEROX SDD	Project: Dove	Floppy Disk Controller - I	File: plOP10.sil	Designer: Tsang	Rev: A	Date: 6/06/84	Page: 10



* *min tRQR = 1.6 us (DMA req to DMA Rd)*
  Delay in 80186 = 5 c.c. = 625 ns.
  So, need to delay 8272 DMA req by ~ 1000 ns.
* *8272 DMA req will go away 200 ns after DMA Ack is presented to 8272.*

Signal Cable Ground



Signal Connector

* *34-pin PCB edge connector. 0.100 inch spacing*
* *Pins 2 & 34 are spare.*
* *Pin 2 is located at the end near the key slot on component side.*
* *All odd numbered pins are ground, located on non-component side.*
* *ScotchFlex P/N 3463-0001 or AMP P/N 583717-5*
* *Signal cable in max 10 ft of ribbon or twisted pair*

Power Connector

* *4 pins Mate-N-Lok connector*
* *AMP P/N 1-480424-0*
* *Pins: AMP P/N 61473-1*
* *Wire: #18 AWG*

+12v = 1, +5v = 4,
GND = 2, 3

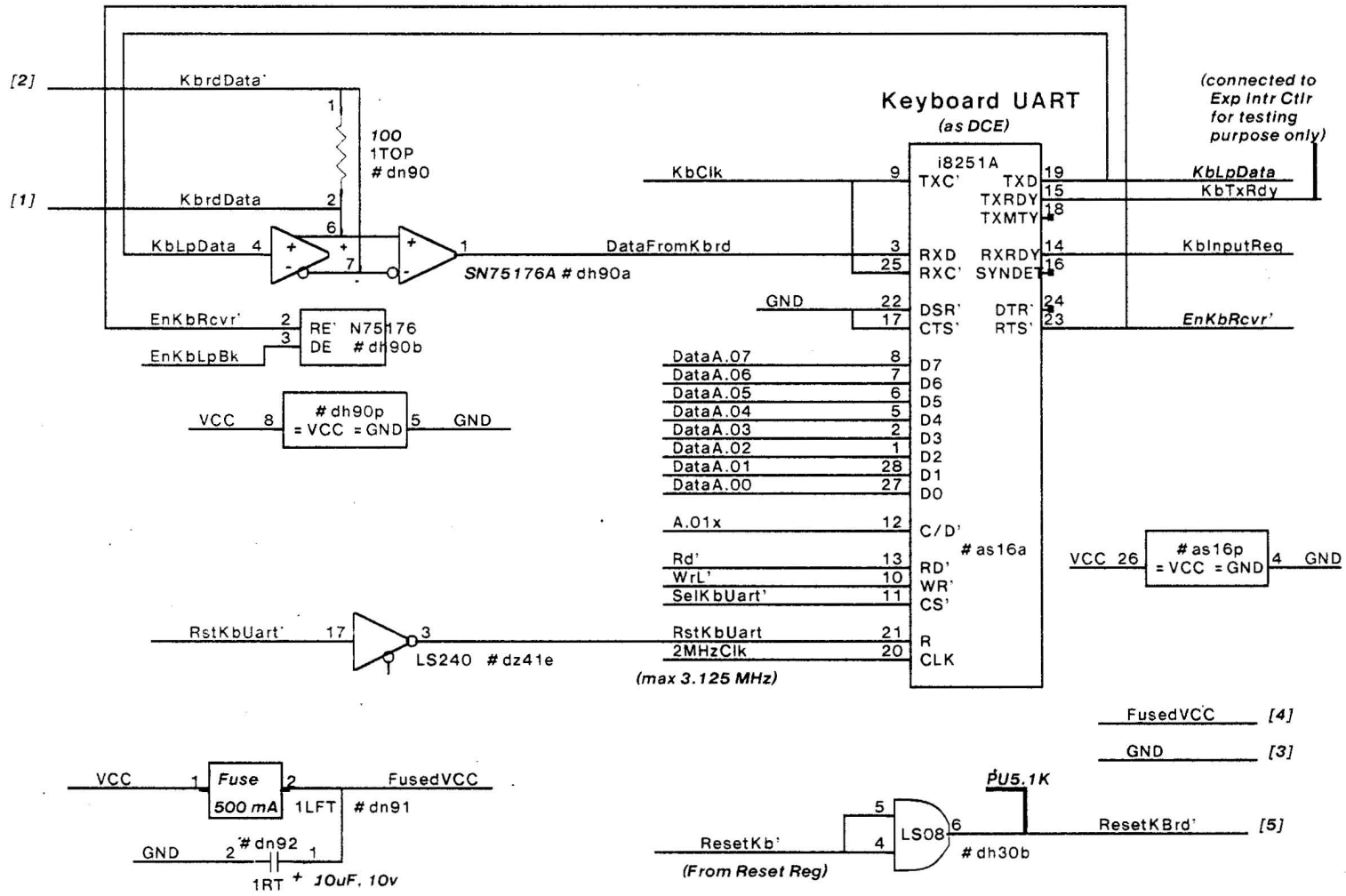
Frame Ground Mating Connector

* *AMP P/N 60972-1*

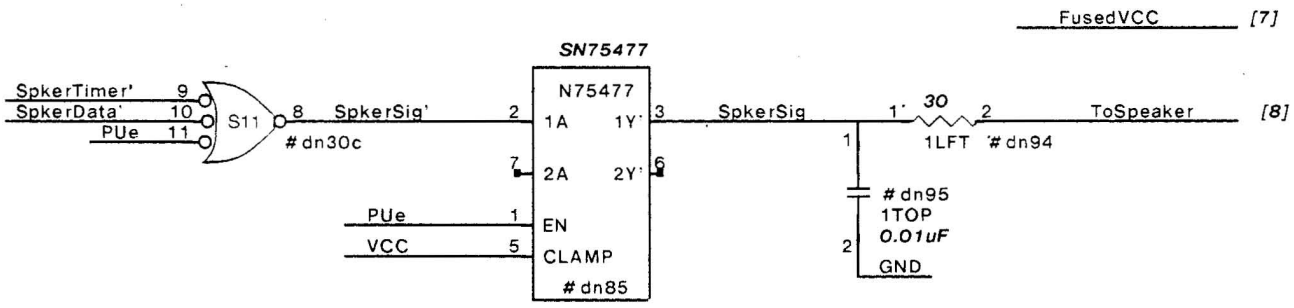
8272b - 0

XEROX SDD	Project: Dove	Floppy Disk Controller - II	File: pIOP11.sil	Designer: Tsang	Rev: A	Date: 6/06/84	Page: 11

Keyboard Interface :



Speaker Interface :



Keyboard Interface :

- *9600 baud*
- *1 start bit, 8 data bits, 1 stop bit. ~ 1 character per ms.*
- *kb takes ~ 10 ms per scan, then take ~ 5 ms to send 1 - 3 bytes of kb/mouse code to IOP.*

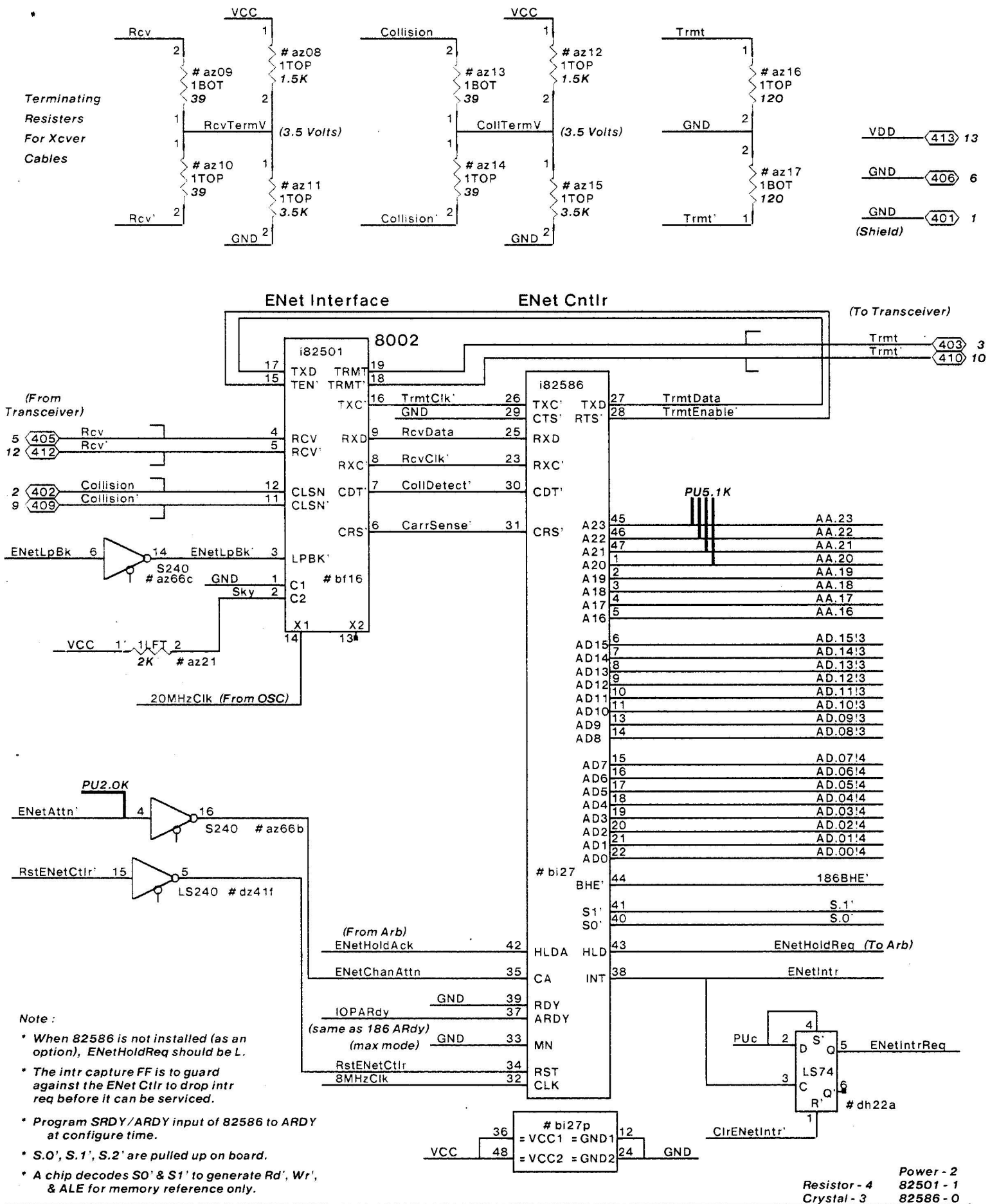
Connector :

KbrdData	1
KbrdData'	2
Gnd	3
Vcc	4
ResetKBrd'	5
unused	6

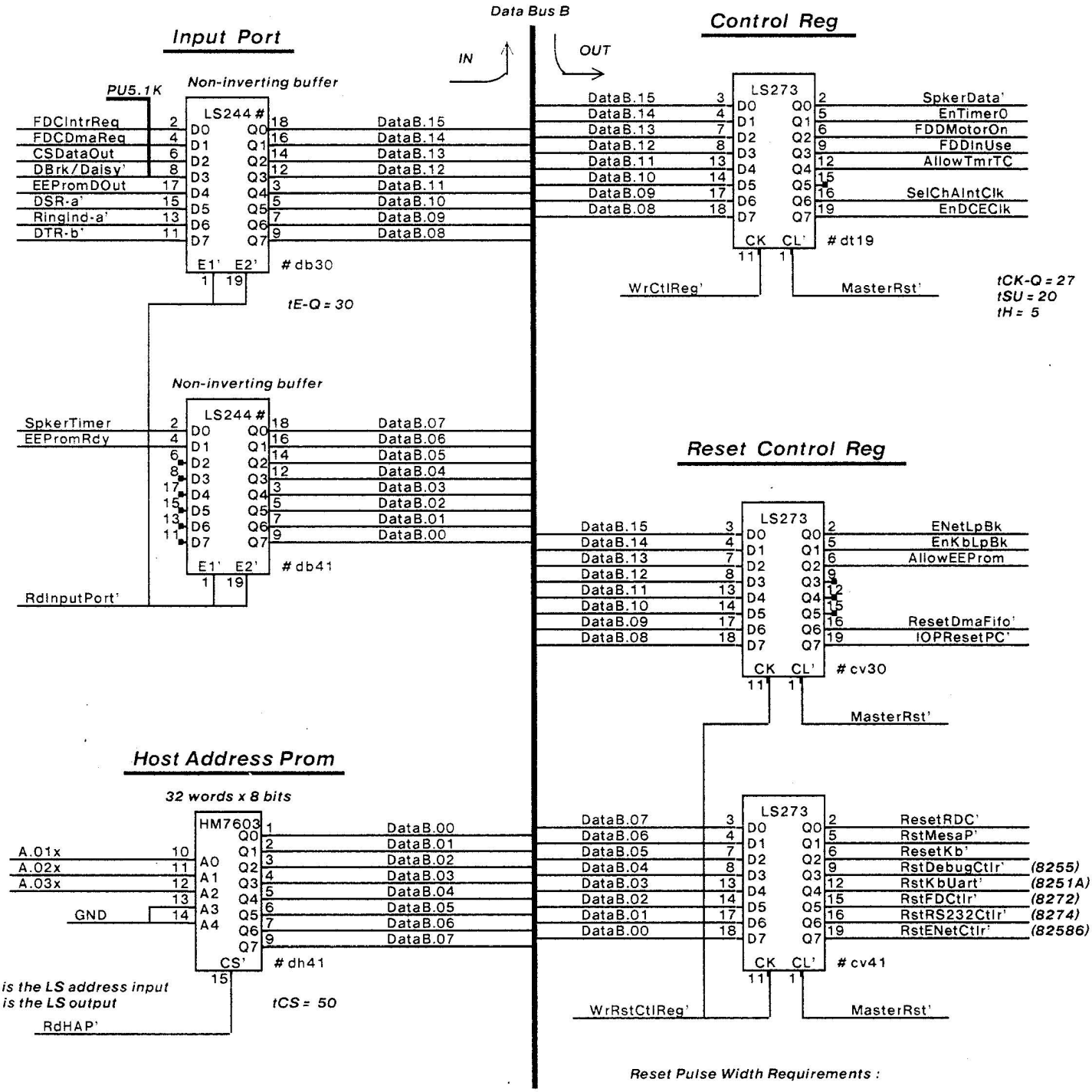
SN75176A RS422A
DS3695 RS485
75157 (R)
75158 (D)

75477 - 9
75176b - 8
75176a - 7
power - 2
8251 - 0

XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dove	Keyboard & Speaker Interfaces	pIOP12.sil	Tsang	A	6/06/84	12



XEROX SDD	Project Dove	Ethernet Controller	File pIOP13.sil	Designer Tsang/Thompson	Rev A	Date 6/06/84	Page 13



Reset Pulse Width Requirements :

* 8255A-5, at least 50 us after power-up ; at least 500 ns for subsequent reset pulses.
* 8272A, 14 tCY = 3.5 us.
* 8274, > 250 ns.
* 8251A, 6 tCY = 3 us.
* 82586,
* 80186, at least 50 us after power up; at least 4 cc = 0.5 us for subsequent resets.
* Mesa chip,
* Keyboard, (8048), active for 50 ms after power-up; 20 us for subsequent resets.

* Host address is 48 bits long, stored in addresses 0 - 5 of the PROM.
* Address 6 contains an 8-bit checksum.
* Address 7 contains the complement of the checksum.

I/O Address	Host Address Bits
90	0 -- 7
92	8 -- 15
94,96,98	/
9A	40 -- 47
9C	Checksum
9E	Checksum'

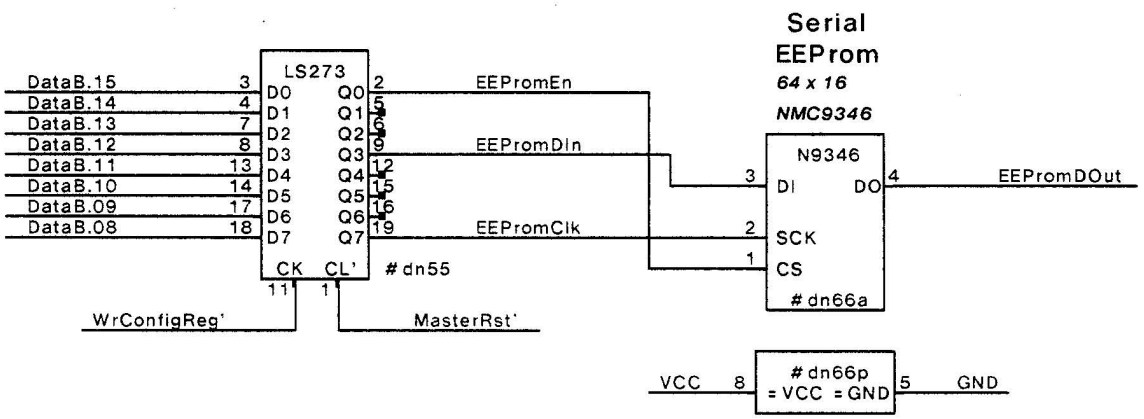
(increment = 02H)

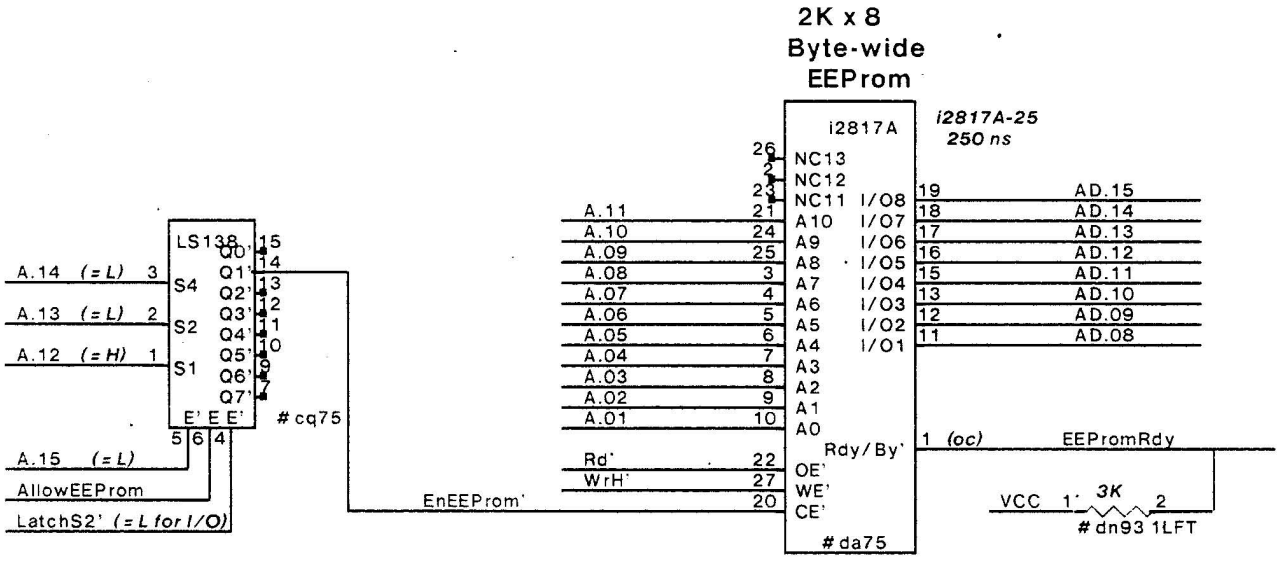
Possible PROMs :

74S288	25 ns
82S123	50 ns
HM7603	50 ns
AMD27S19	40 ns

74244 - 1
74240 - 0

XEROX SDD	Project Dove	Input Port, Control Reg, Reset Control Reg, & HAP	File plOP14.sil	Designer Tsang	Rev A	Date 6/05/84	Page 14





tACC = 250
tCE = 250
tOE = 100
tDF = 60
min tWP = 100
Write Cycle = 20 ms max

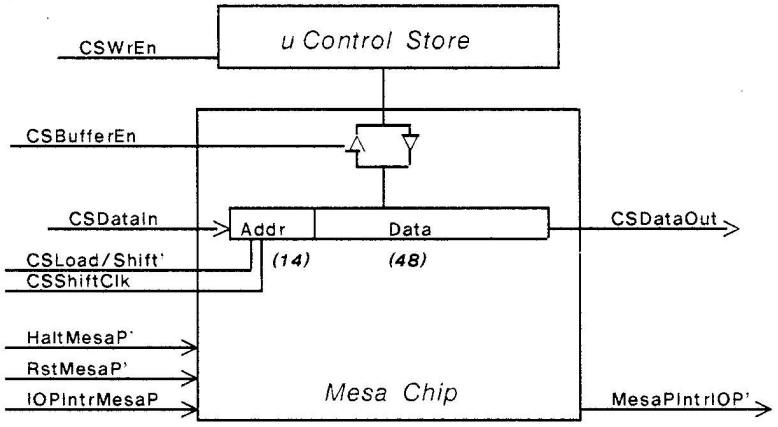
* *EEProm locates at I/O addresses 1000H - 1FFFH (second lower 4K region)*
* *10,000 Erase/Write cycle*
* *10 yrs data retention*
* *On-chip sensing circuit disables internal programming if VCC falls below 4V.*

2817A - 3
power - 2
9346 - 1

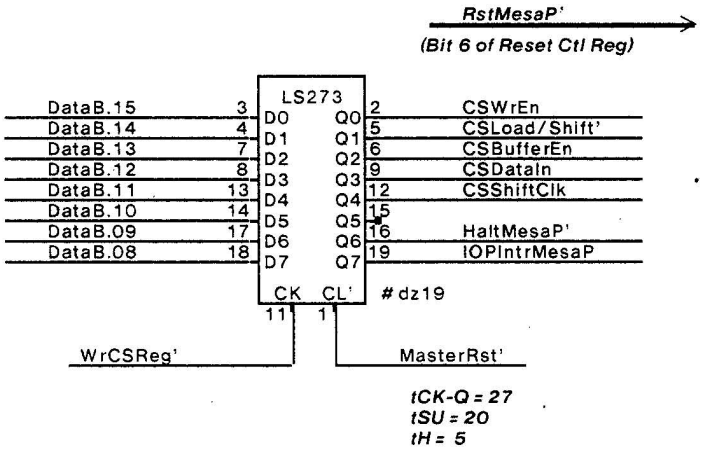
XEROX SDD	Project: Dove	System Configuration EEProm	File: pIOP15.sil	Designer: Tsang	Rev: A	Date: 6/04/84	Page: 15

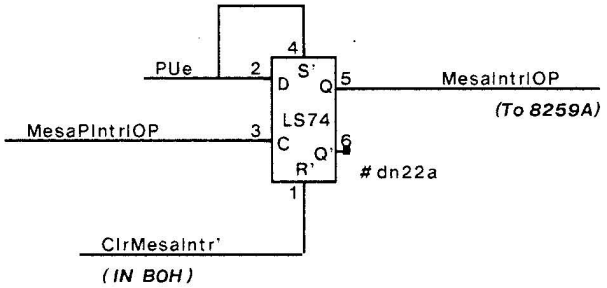
Mesa Processor & Control Store Interface

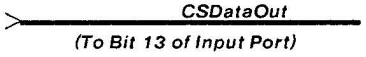
Block Diagram :



Note : Shift Reg shifts on L-to-H transition of clock.

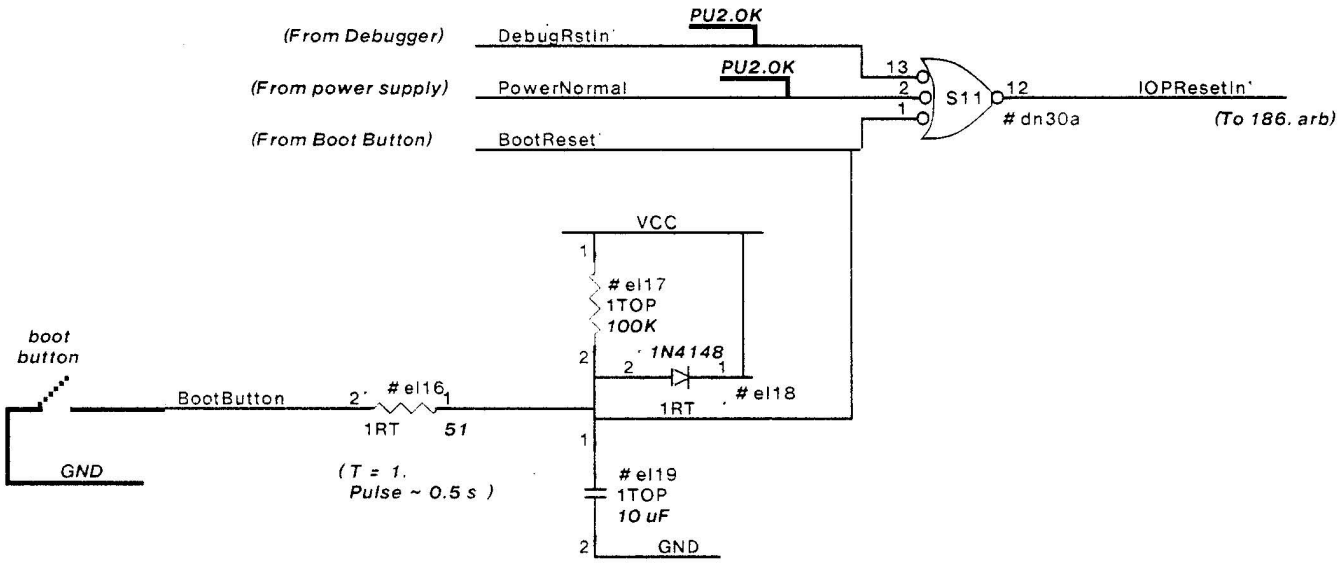






XEROX SDD	Project Dove	Mesa Processor & Control Store Interface Logic	File plOP16.sil	Designer Tsang	Rev A	Date 6/04/84	Page 16

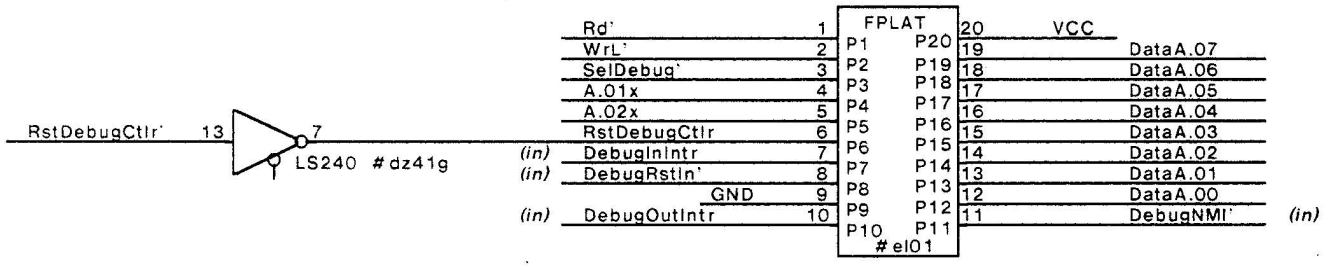
Reset Logic :



Note : 1. 186ResetIn' should go H no sooner than 50 us after power up.
2. 186ResetIn' is required to be low for > 4 c.c. = 0.5 us.
3. 186 begins fetching inst ~ 7 c.c. after 186ResetIn' goes H.

PowerNormal becomes H btwn 50 - 250 ms after all power supply outputs have exceeded 94 % of nominal.

Debugger Cable Interface :

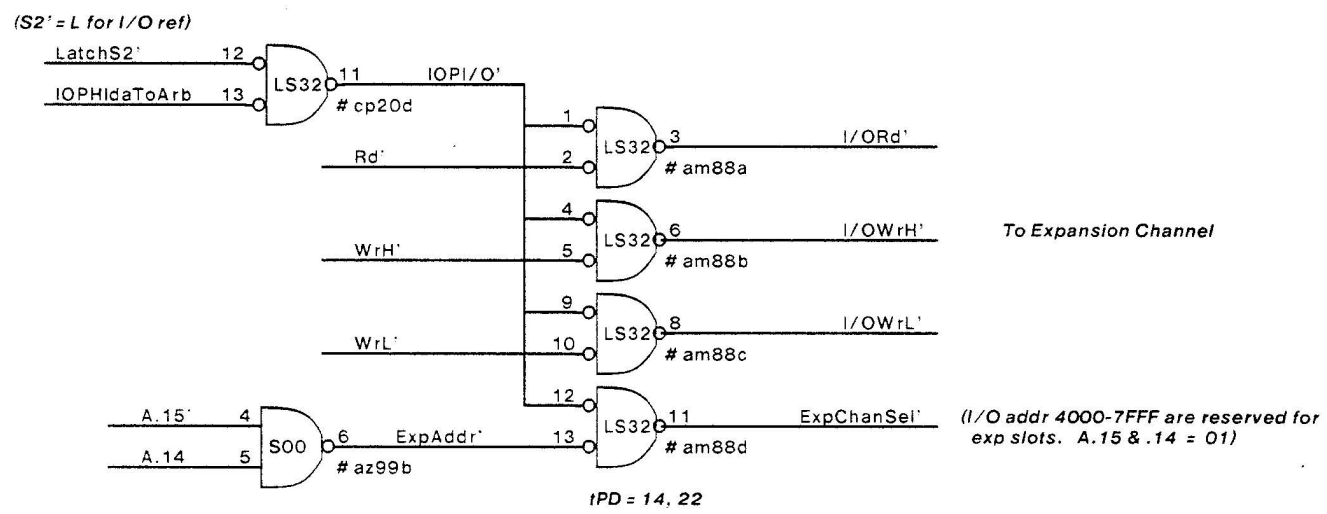


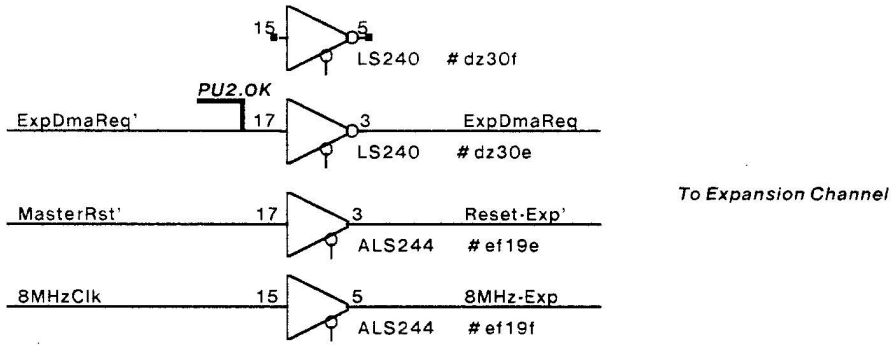
DebugInIntr = => 8255 to 80186

DebugOutIntr = => 80186 to 8255

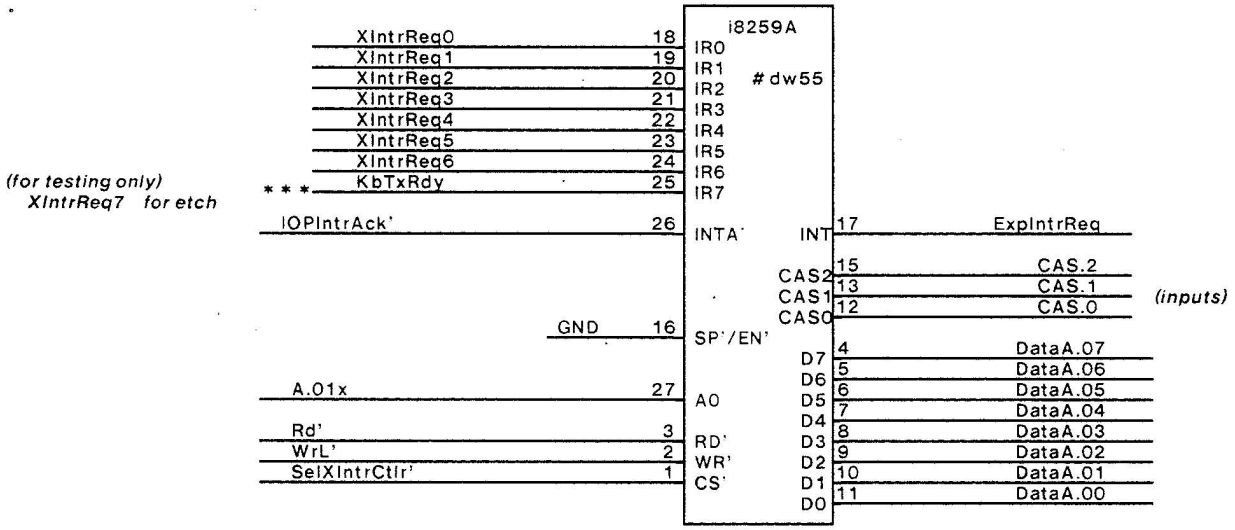
Resistor - 3
Plat18 - 2
Diode - 1
Switch - 0

XEROX SDD	Project Dove	Reset Logic & Debugger Interface	File plOP17.sil	Designer Tsang	Rev A	Date 6/06/84	Page 17





Exp Chan Intr Ctlr

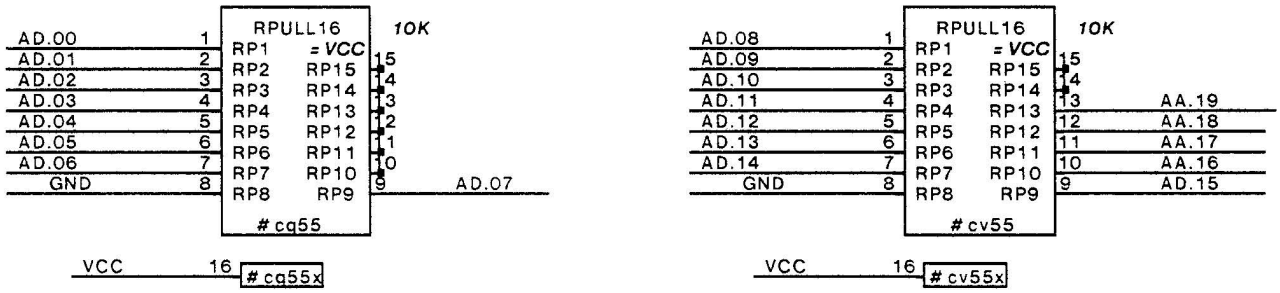


Resistor - 1
8259 - 0

XEROX SDD	Project Dove	Expansion Channel Interface	File pIOP18.sil	Designer Tsang	Rev A	Date 6/04/84	Page 18

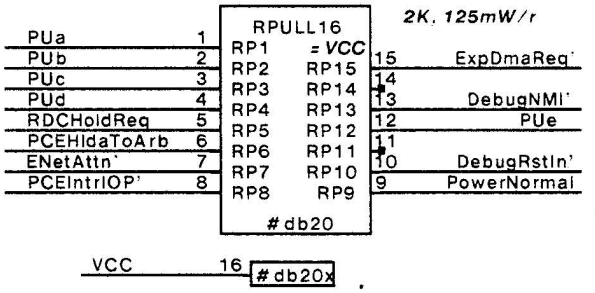
This page is incomplete

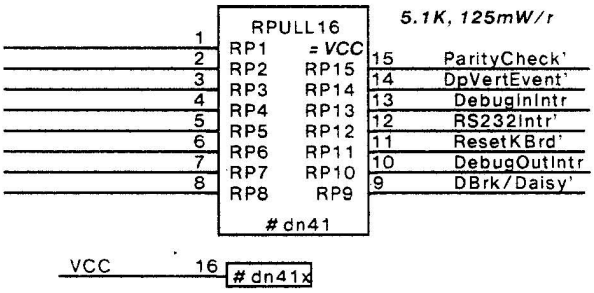
AD - Bus Pull-up R's

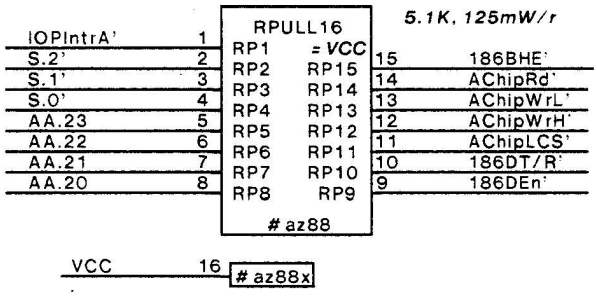


Note: If want to pull-up 186 AD-Bus, can insert 10K R-paks into these two sockets.

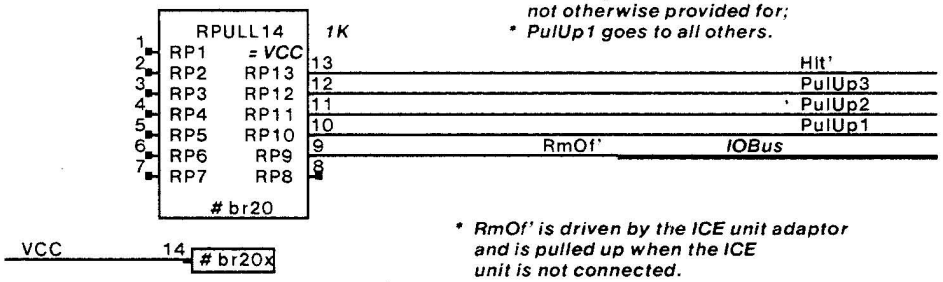
Misc Pull-up R's







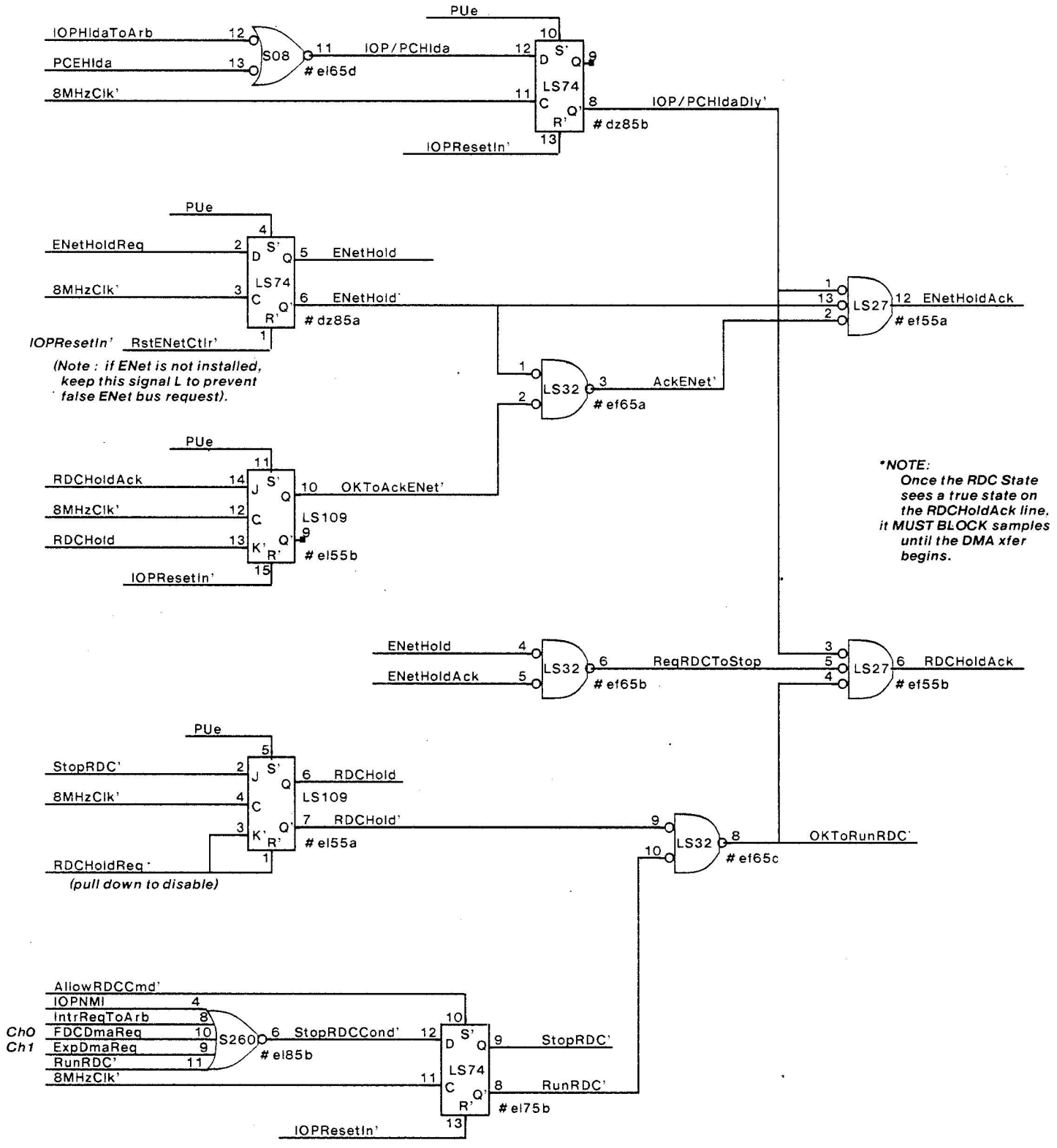
DMA/RDC :



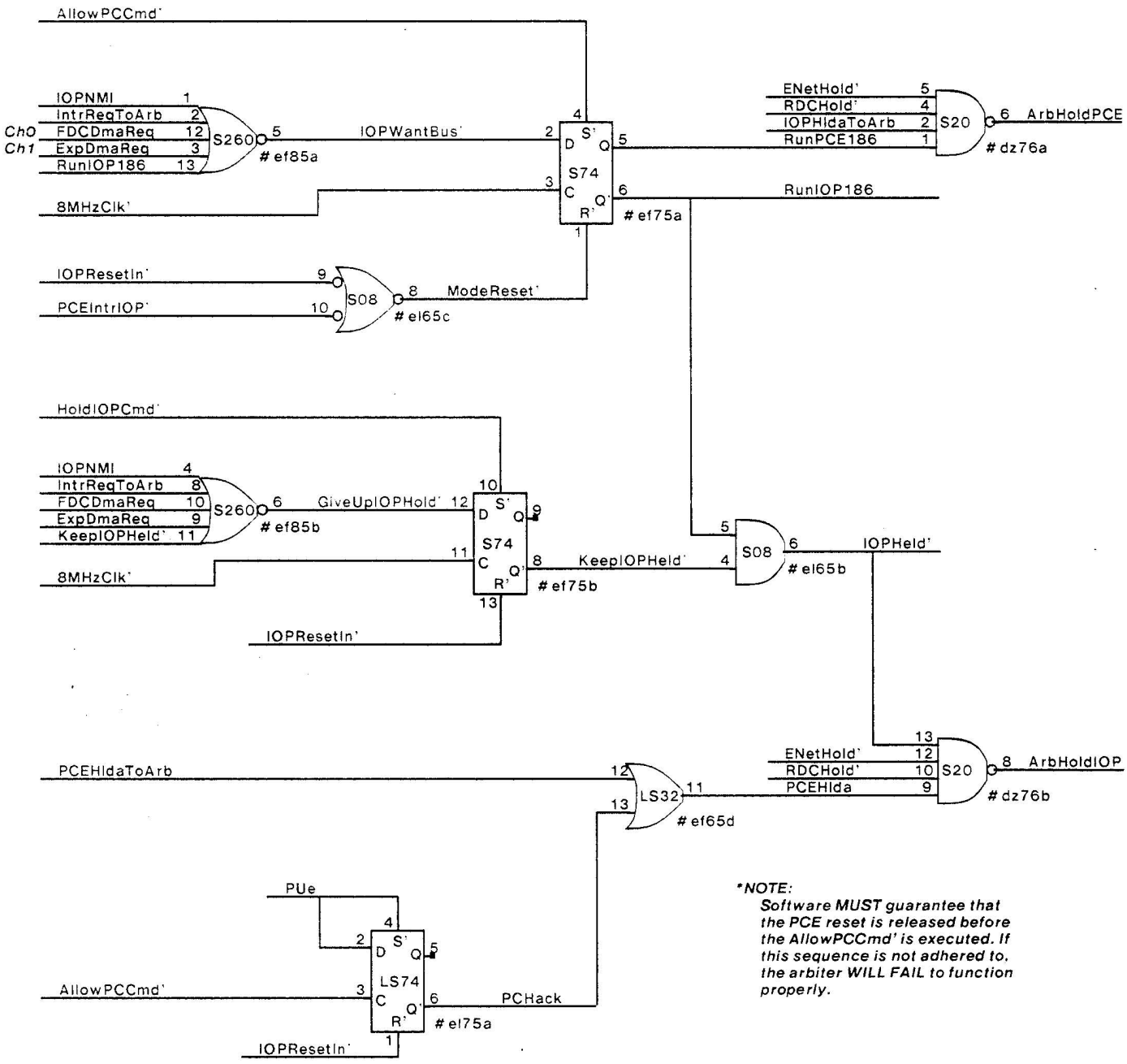
* *PulUp3 goes to clear' & reset' inputs not otherwise provided for;*
* *PulUp2 goes to set inputs not otherwise provided for;*
* *PulUp1 goes to all others.*

* *RmOf' is driven by the ICE unit adaptor and is pulled up when the ICE unit is not connected.*

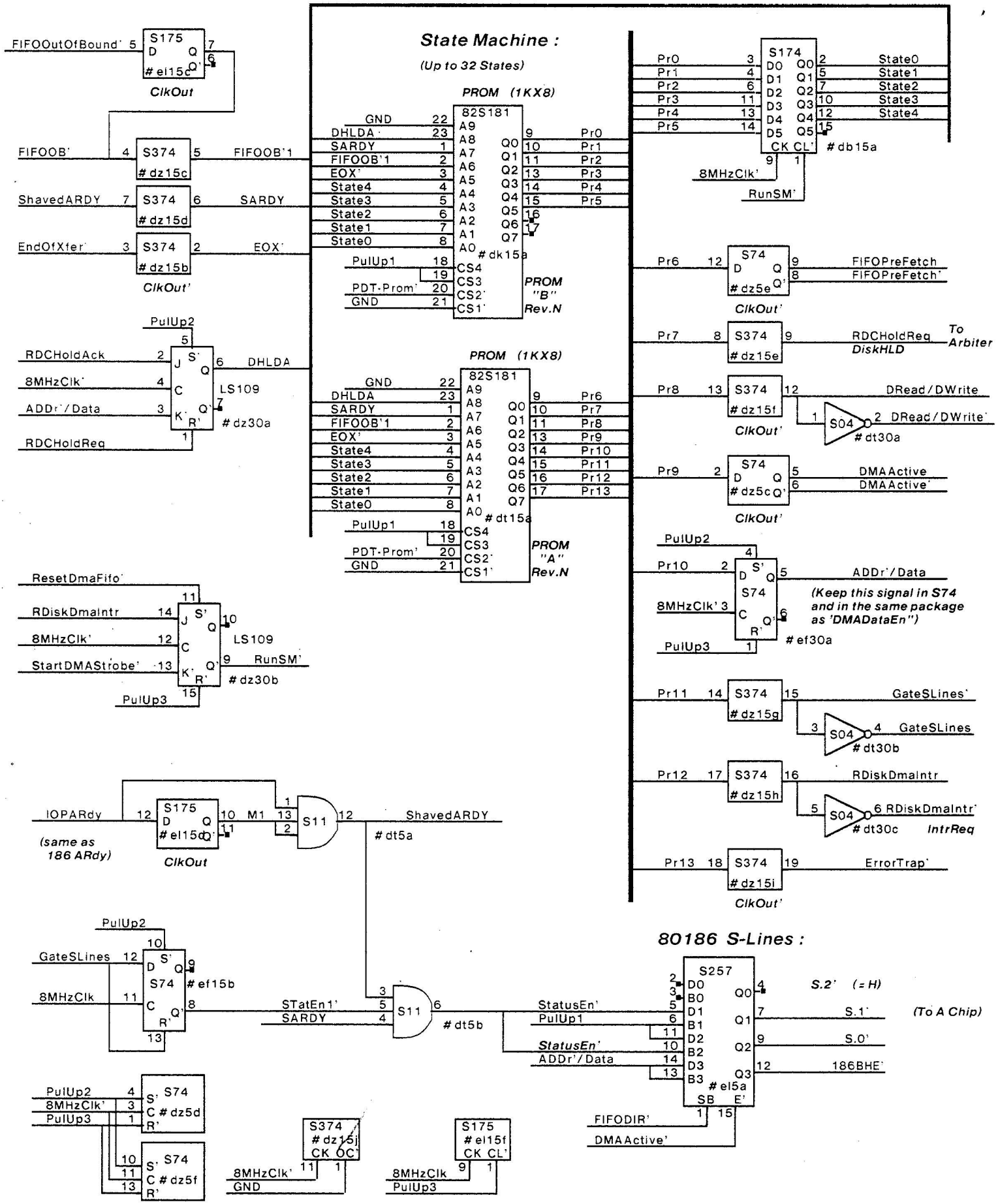
XEROX SDD	Dove	Pull-up Resistors & Misc	File: pIOP19.sil	Designer: Tsang	Rev: A	Date: 6/04/84	Page: 19



XEROX SDD	Project Dove	Arbitration Logic	File plOP20.sil	Designer R. Knauss	Rev A	Date 6/06/84	Page 20

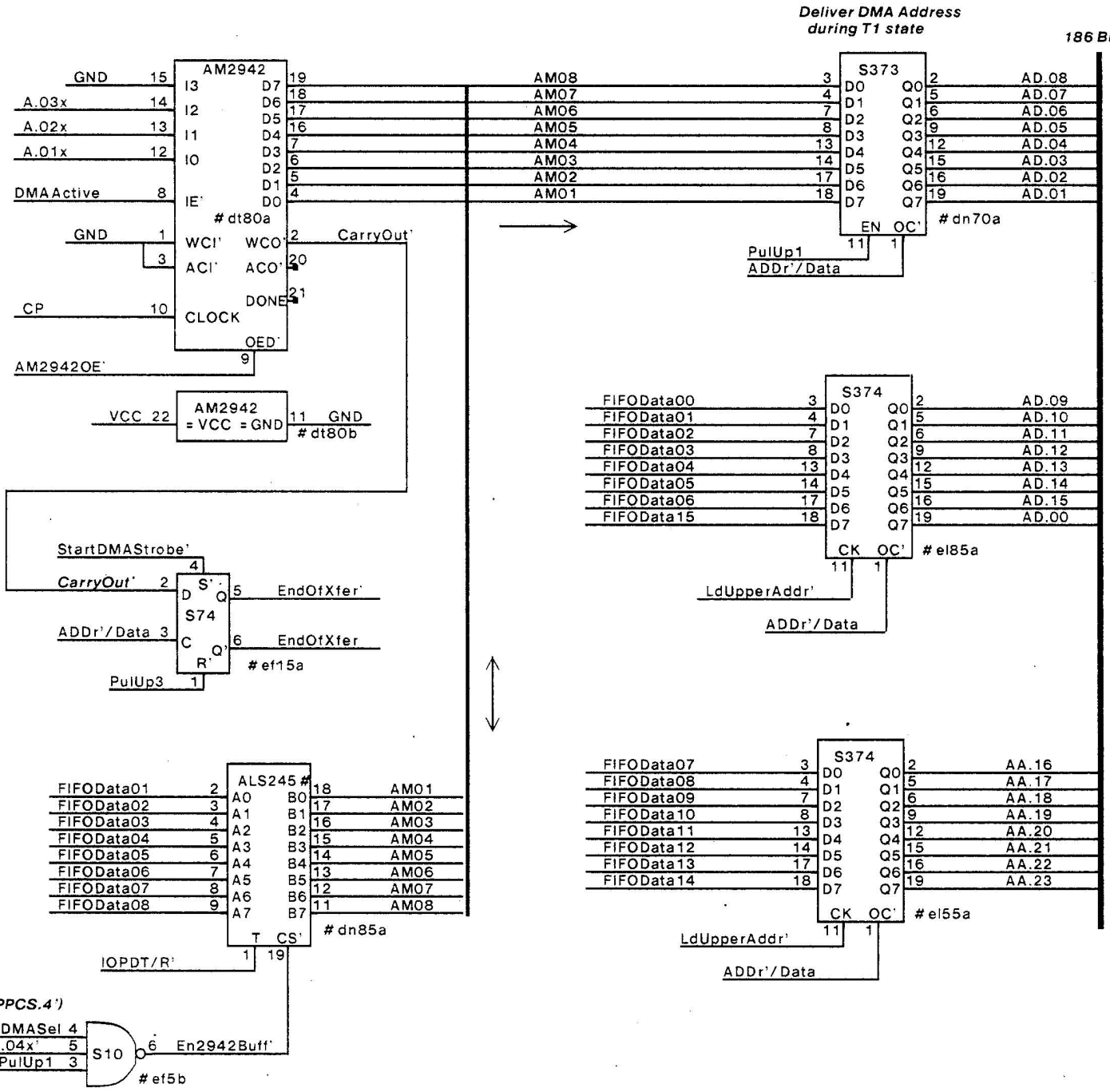


XEROX SDD	Project Dove	Mode Control Logic	File pIOP21.sil	Designer R. Knauss	Rev A	Date 6/04/84	Page 21



82S181 - 1

XEROX SDD	Project: Dove	DMA State Machine & S - Lines	File: plOP22.sil	Designer: Oloumi	Rev: A	Date: 6/06/84	Page: 22



Notes:

CP at ↑ will count/load

IO Address:
A04-01 = 0XXX All for 2942 i.e.

0000 Write CR2-CR0
0001 Read CR2-CR0
0010 Read Word Counter
0011 Read Addr Counter
1000 DMA CMD/Status
1001 Preset A1' (Write only)
1010 CTL CMD/Status
1011 Start DMA (write only)

0100 Re-initialize Counters and Load Address (bits 23-9&0)
0101 Load Address (bits 8-1)
0110 Load Word Count
0111 En Counters (don't use)

DMA Starting Address is given by two writes into the registers:
A04-A01 = 0101 Loads bits 8-1 of the starting address (inside the AM2942).
A04-A01 = 0100 Loads bits 23-9 (given over bits 14-00 of the DATA bus).
Bit 15 of data is routed as bit 0 of Starting Address.

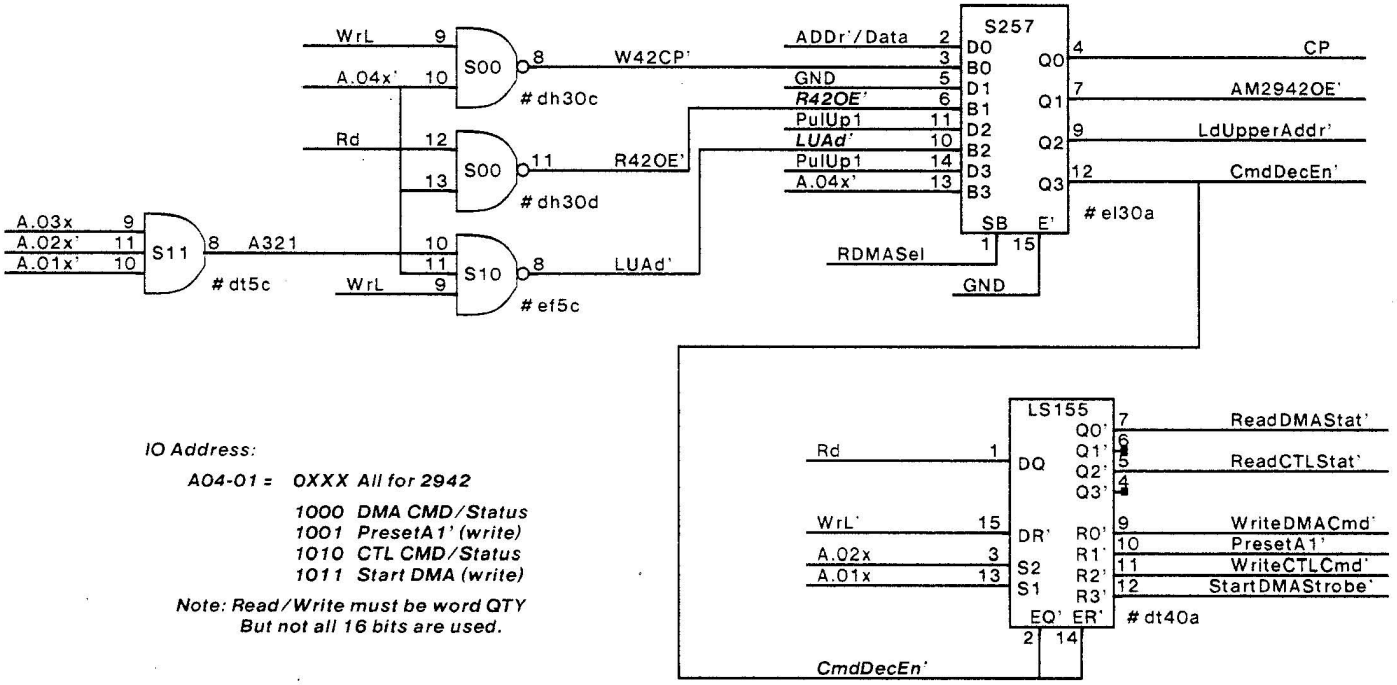
DMA Starting address is not readable by IOP
Writing the Upper address bits (23-9) will also re-initialize the Word Counter and Address Register bits 8-1.

Power Box - 0
S373 - 1

AM2942 - 2
LS245# - 3
LS244# - 4

XEROX SDD	Project: Dove	DMA Address Generation	File: plOP23.sil	Designer: Oloumi	Rev: A	Date: 6/06/84	Page: 23

186 Address Decode



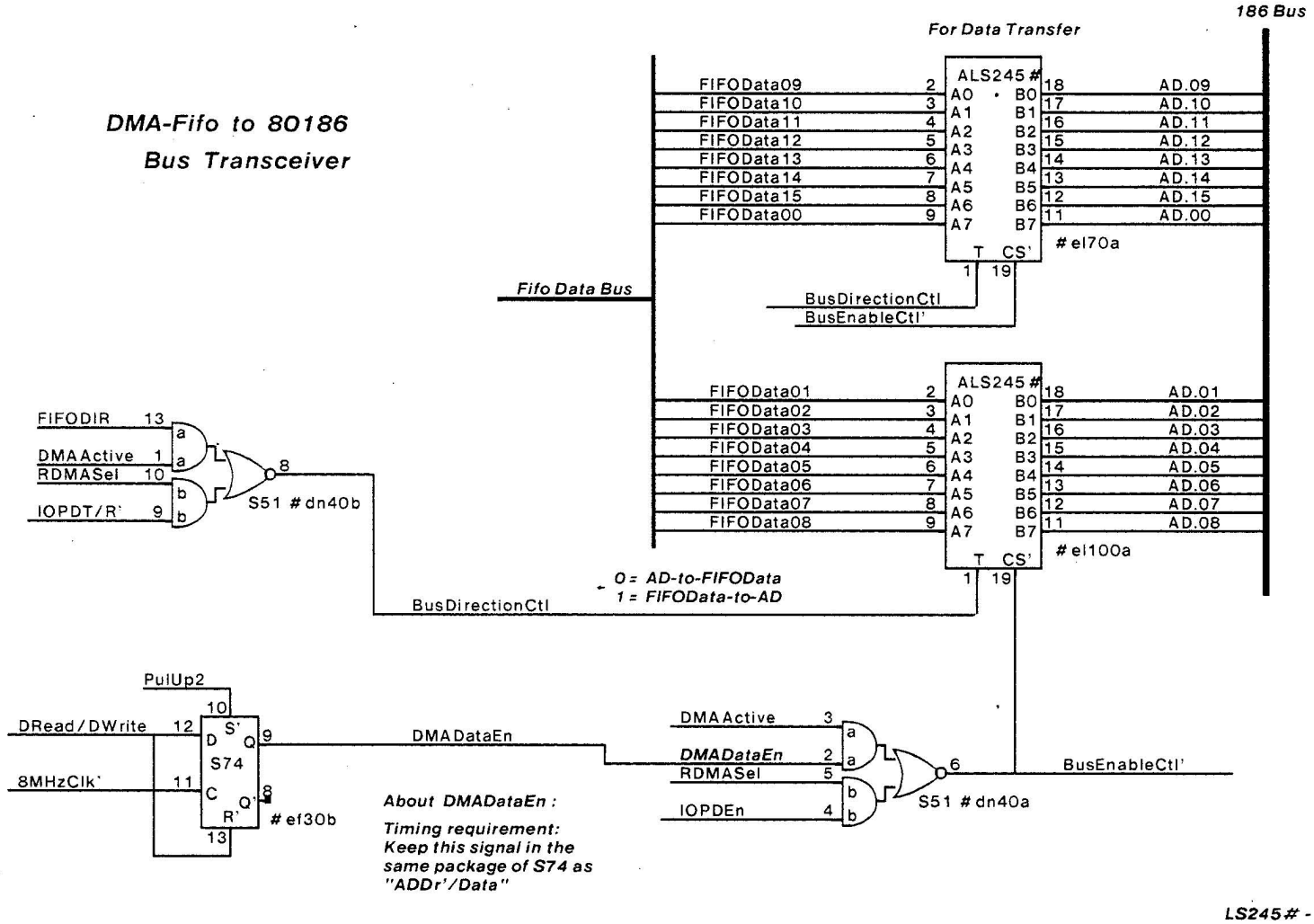
IO Address:

A04-01 = 0XXX All for 2942

1000 DMA CMD/Status
1001 PresetA1' (write)
1010 CTL CMD/Status
1011 Start DMA (write)

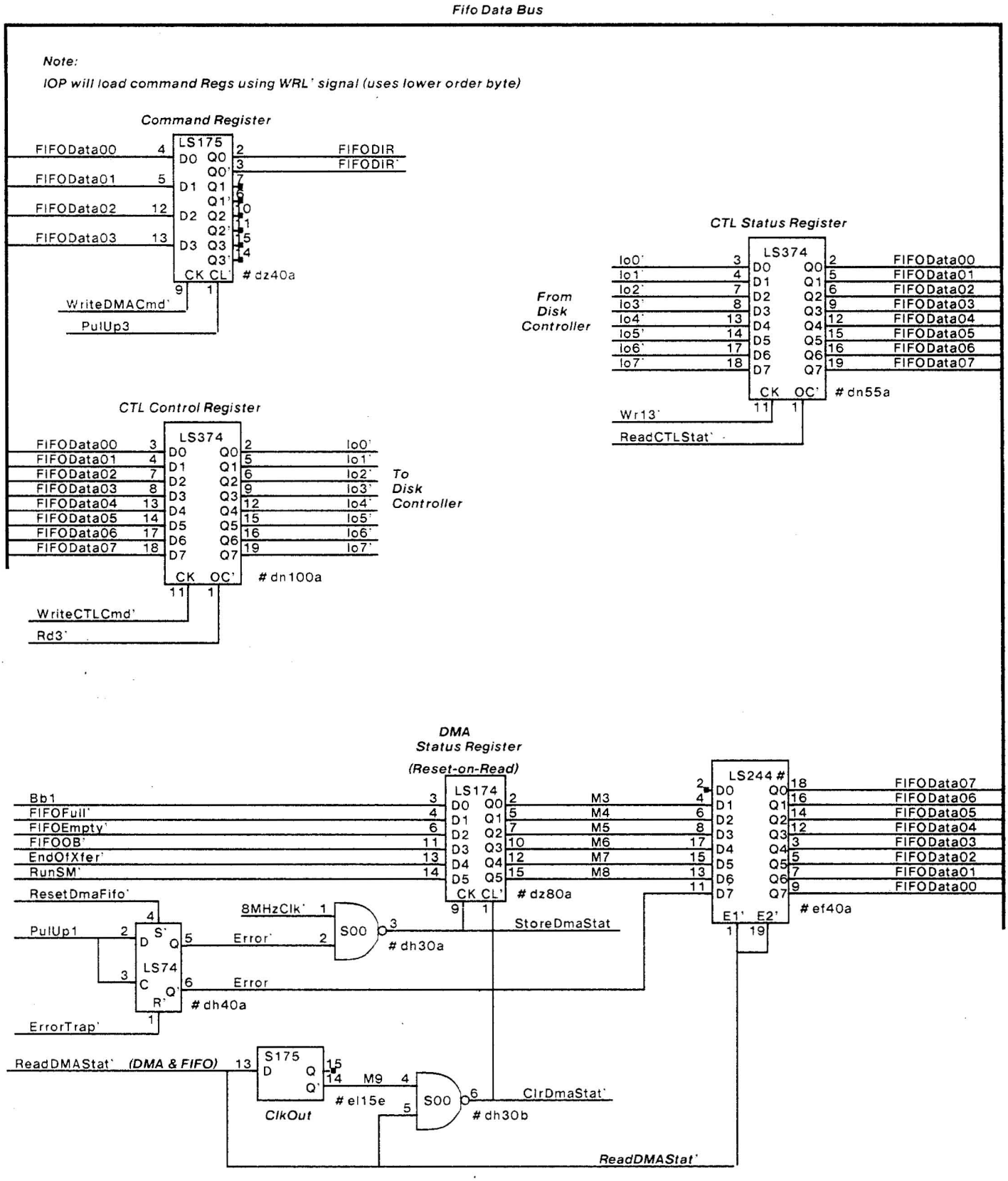
Note: Read/Write must be word QTY
But not all 16 bits are used.

DMA-Fifo to 80186 Bus Transceiver



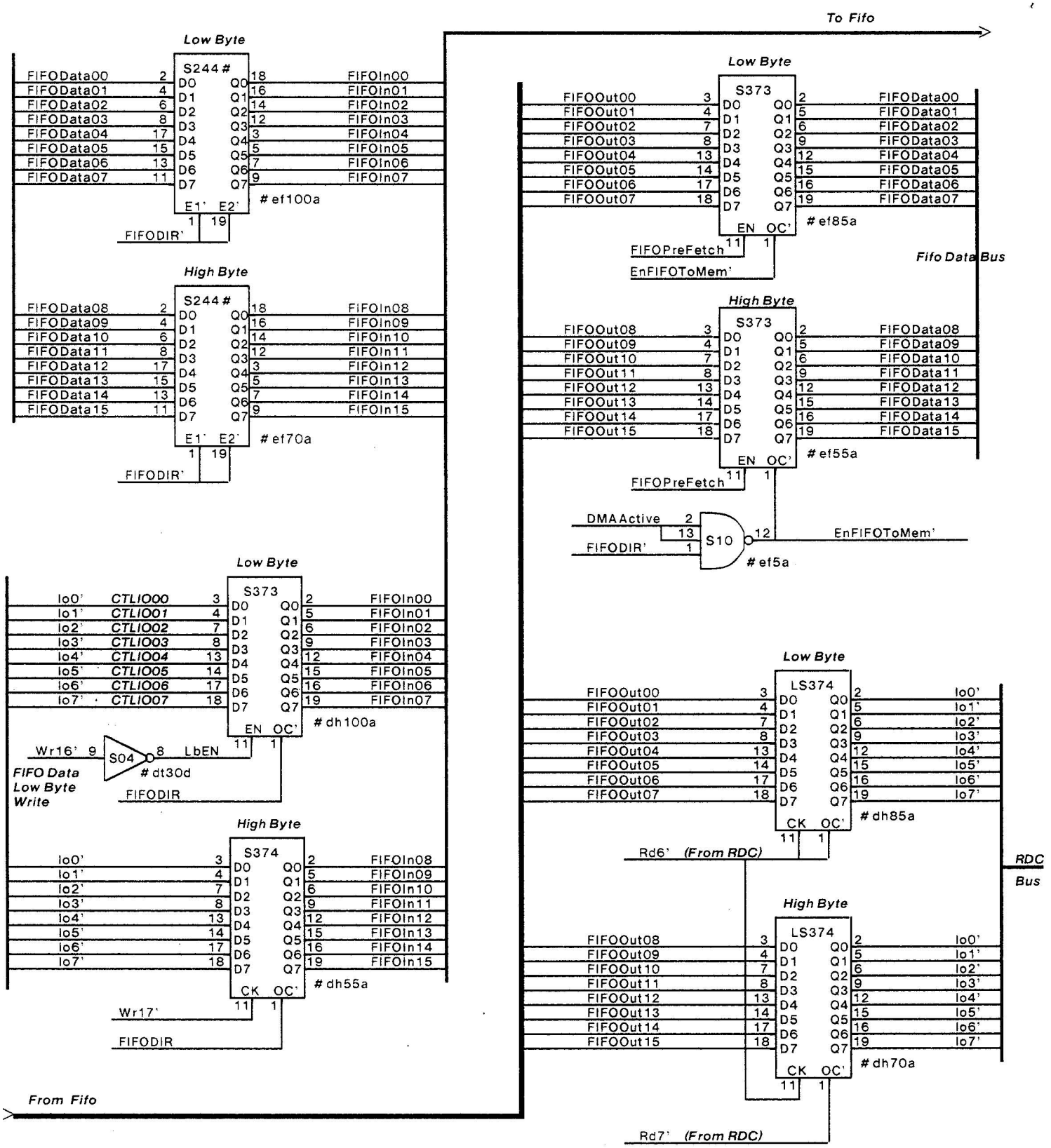
LS245# - 1

XEROX SDD	Project Dove	DMA - 80186 Interface & 186 I/O Address Decode	File pIOP24.sil	Designer Oloumi	Rev A	Date 6/06/84	Page 24



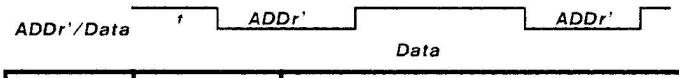
LS244# - 4

XEROX SDD	Project Dove	DMA Command & Status Registers	File pIOP25.sil	Designer Oloumi,Swenson	Rev A	Date 6/06/84	Page 25



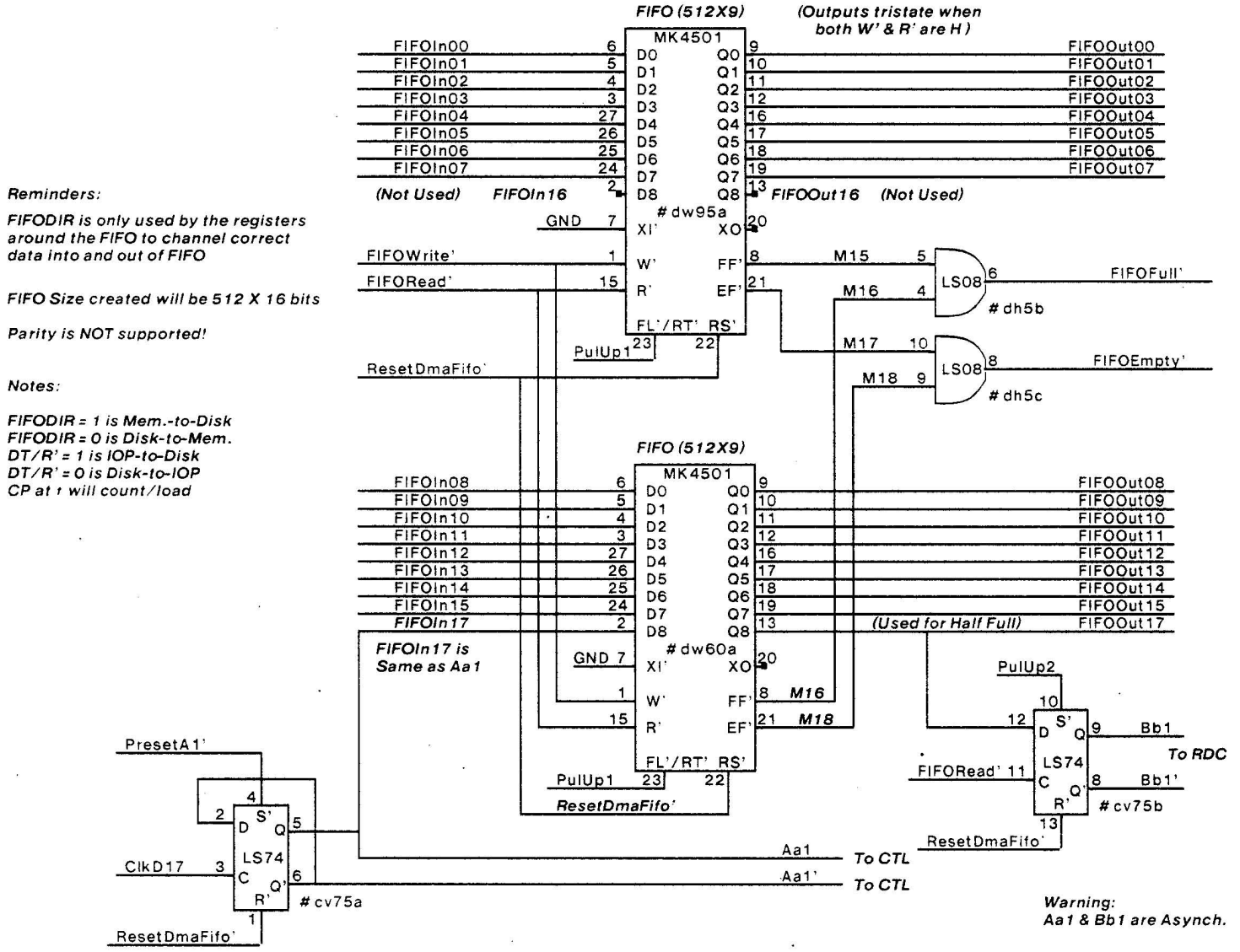
Notes:
FIFODIR = 1 is Mem.-to-Disk
FIFODIR = 0 is Disk-to-Mem.
DT/R' = 1 is IOP-to-Disk
DT/R' = 0 is Disk-to-IOP
CP at ↑ will count/load

←'Reminder: State Machine assures the timing for DRead' & DWrite' (with respect to ADDr'/Data)



S373 - 1
LS244 # - 4

XEROX SDD	Project Dove	Fifo Input & Output Regs	File plOP26.sil	Designer Oloumi	Rev A	Date 6/06/84	Page 26



Reminders:

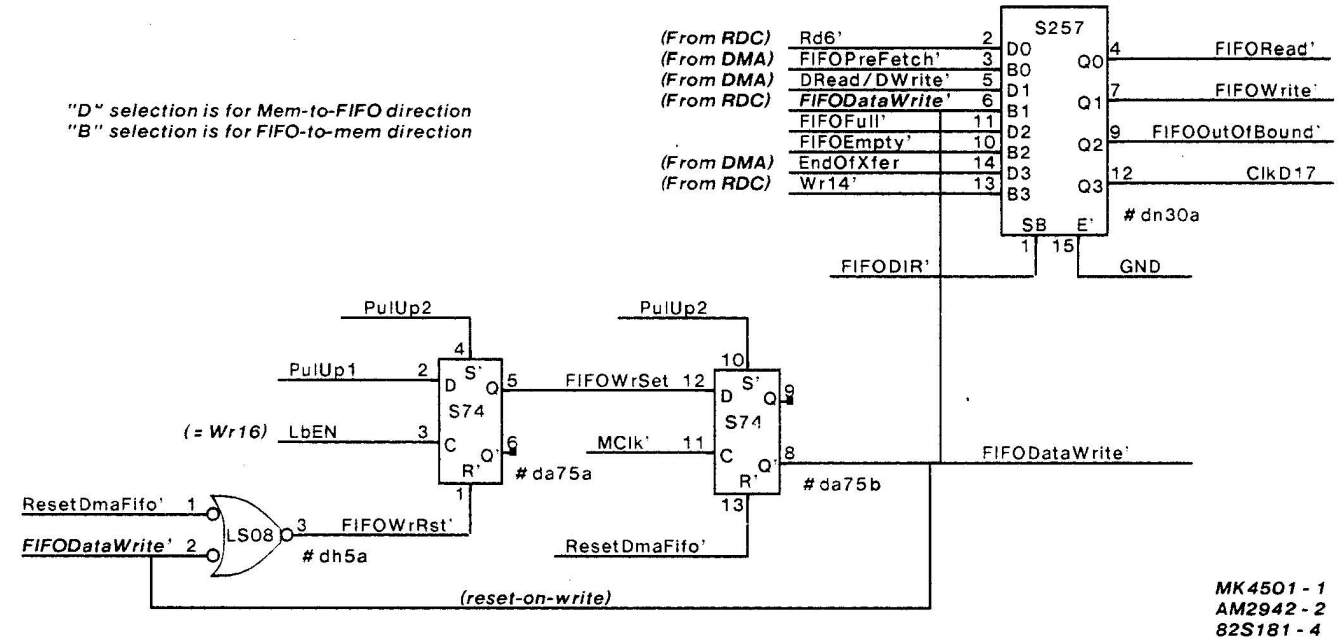
FIFODIR is only used by the registers around the FIFO to channel correct data into and out of FIFO

FIFO Size created will be 512 X 16 bits

Parity is NOT supported!

Notes:

FIFODIR = 1 is Mem.-to-Disk
FIFODIR = 0 is Disk-to-Mem.
DT/R' = 1 is IOP-to-Disk
DT/R' = 0 is Disk-to-IOP
CP at ↑ will count/load

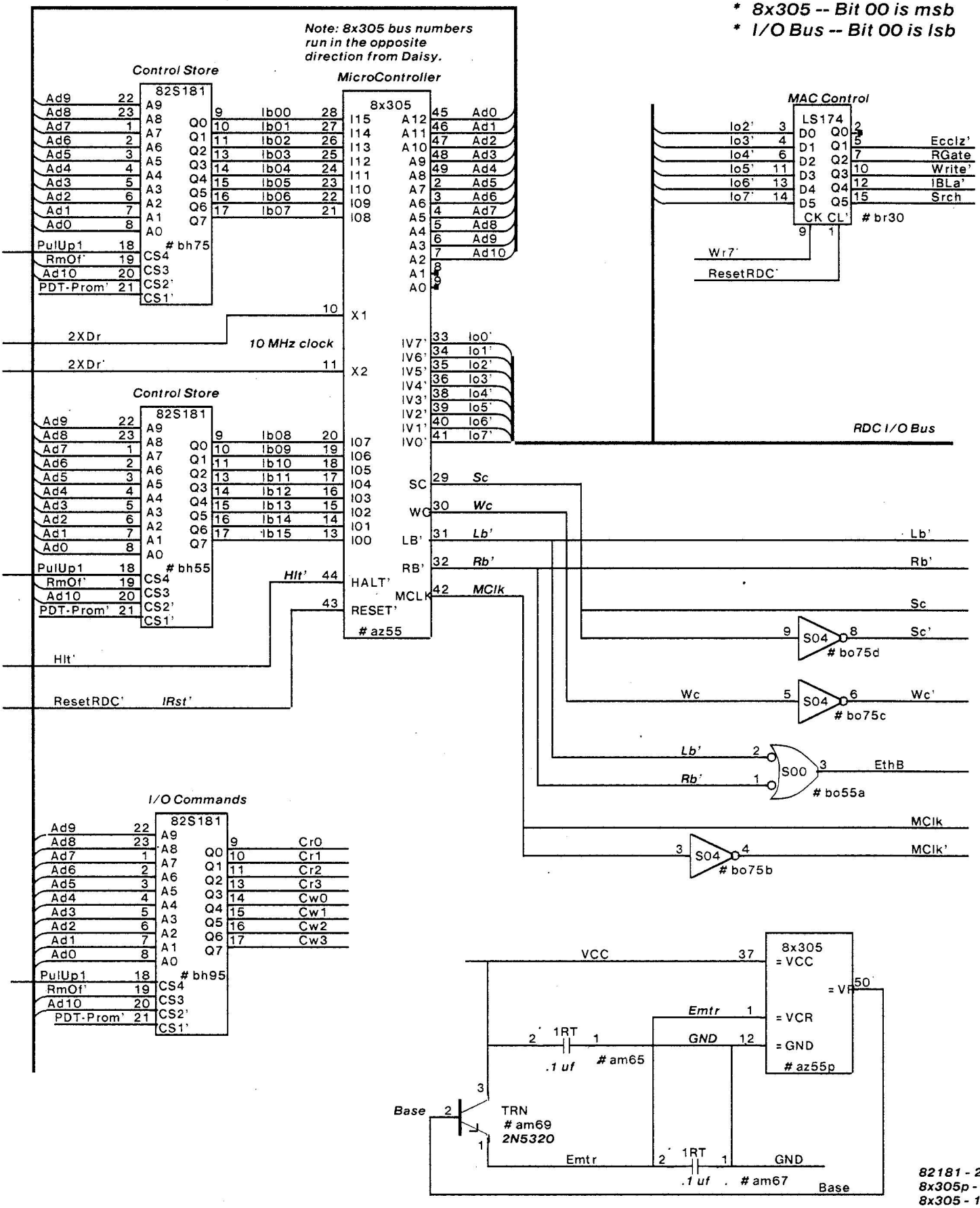


MK4501 - 1
AM2942 - 2
82S181 - 4

XEROX SDD	Project Dove	Fifo Logic	File pIOP27.sil	Designer Swenson,Oloumi	Rev A	Date 6/06/84	Page 27

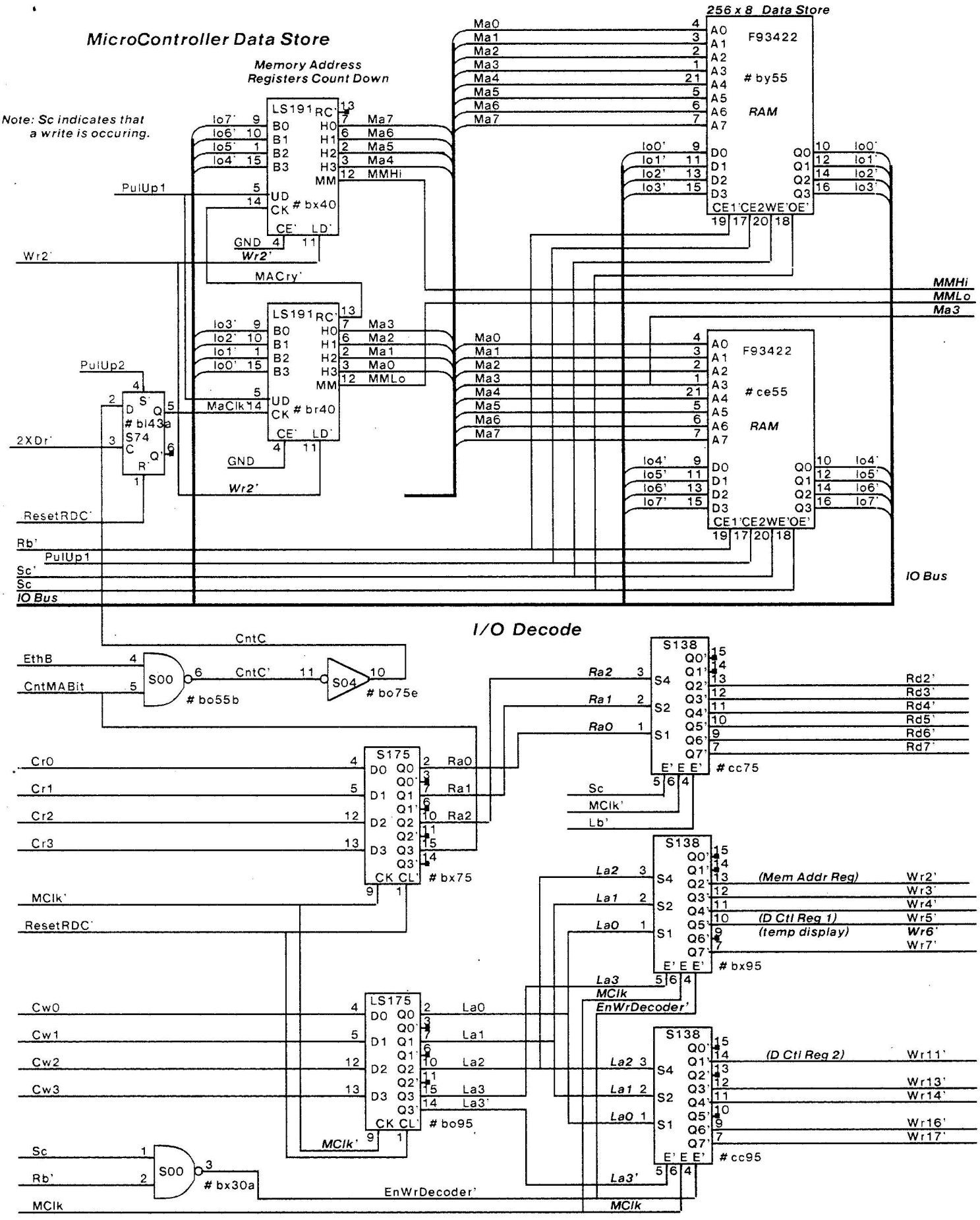
MicroController Section :

Note :
* 8x305 -- Bit 00 is msb
* I/O Bus -- Bit 00 is lsb

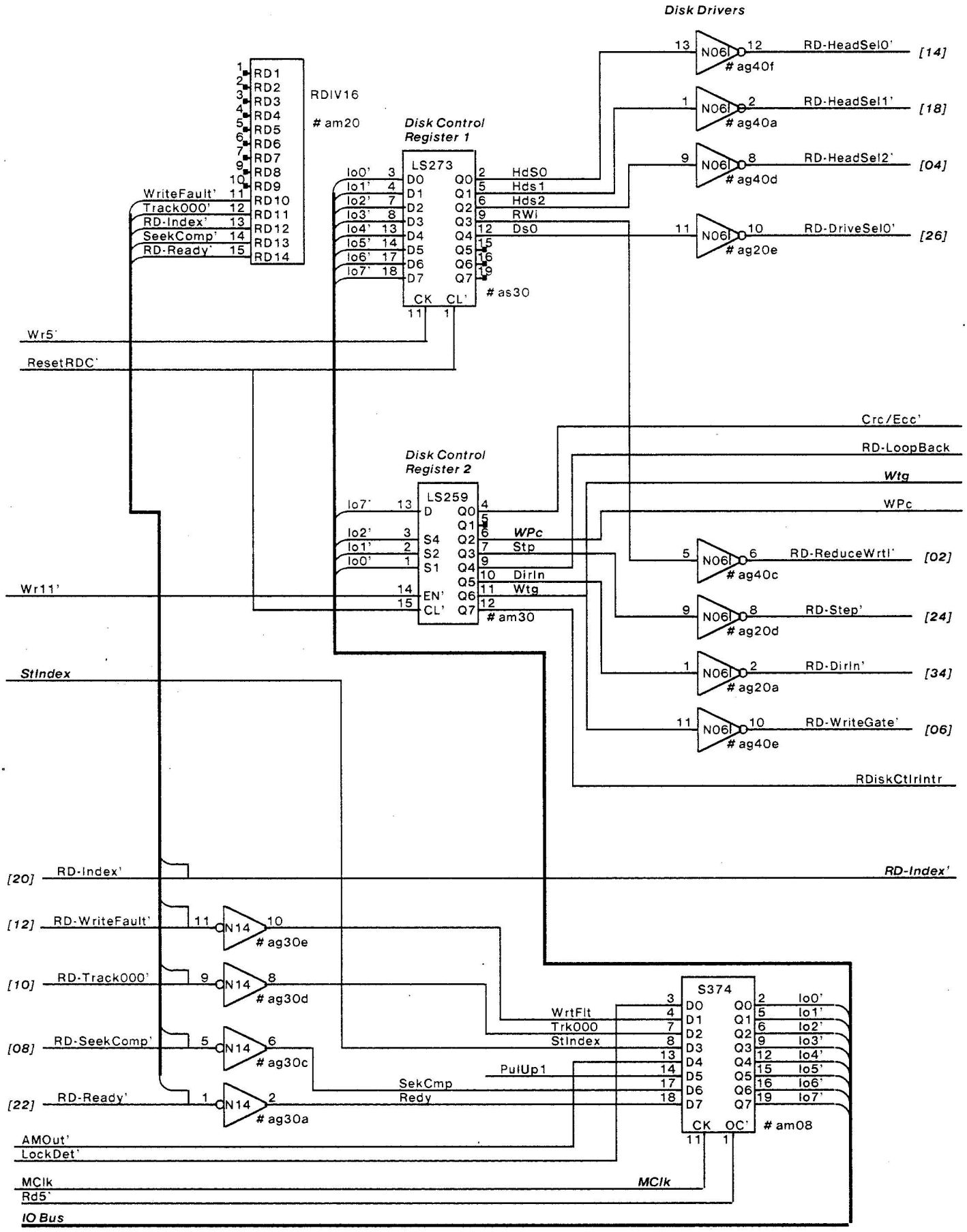


82181 - 2
8x305p - 6
8x305 - 1

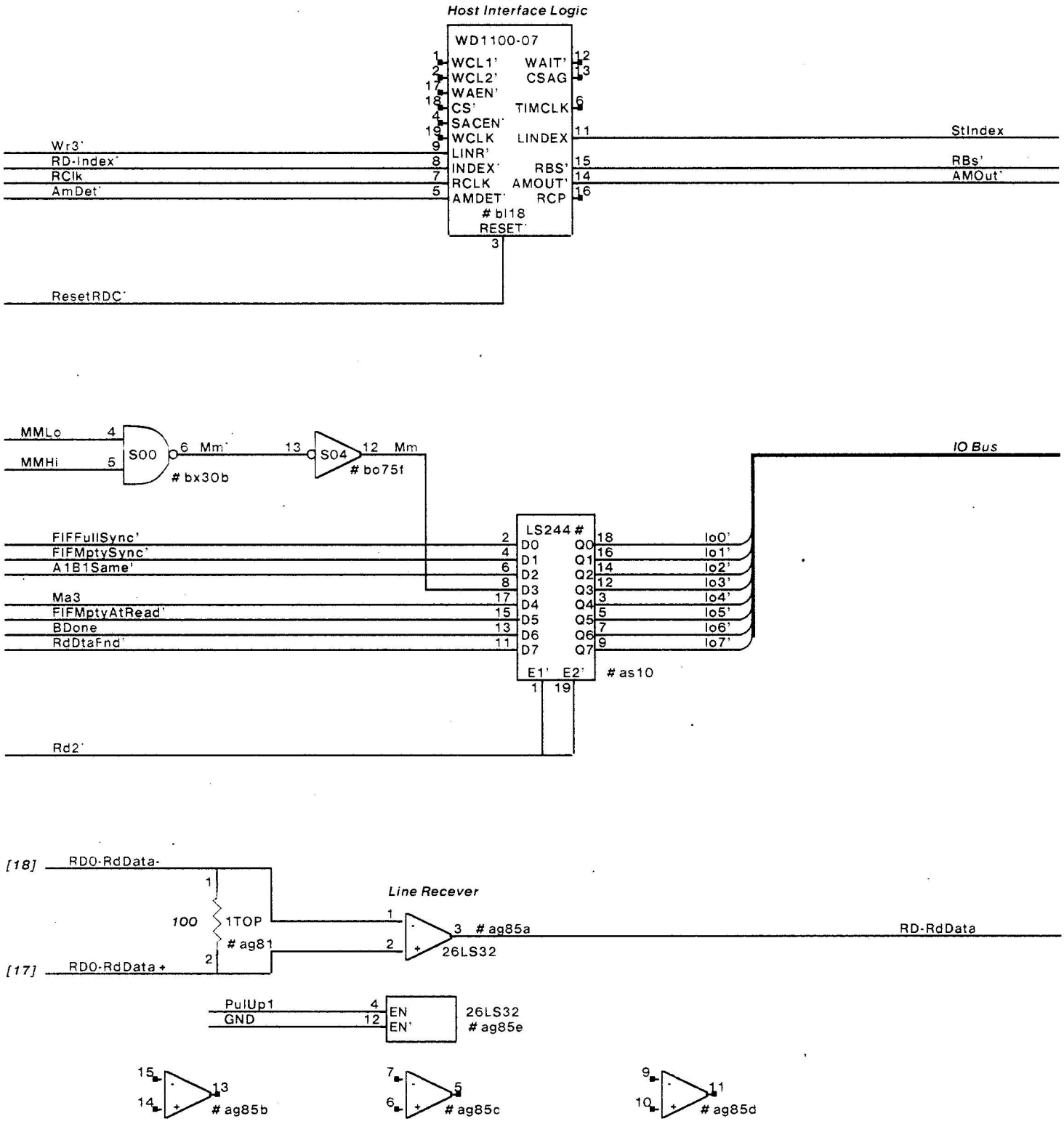
XEROX SDD	Project Dove	8x305 MicroController & Control Store	File pIOP28.sil	Designer Swenson, Oloumi	Rev A	Date 6/04/84	Page 28



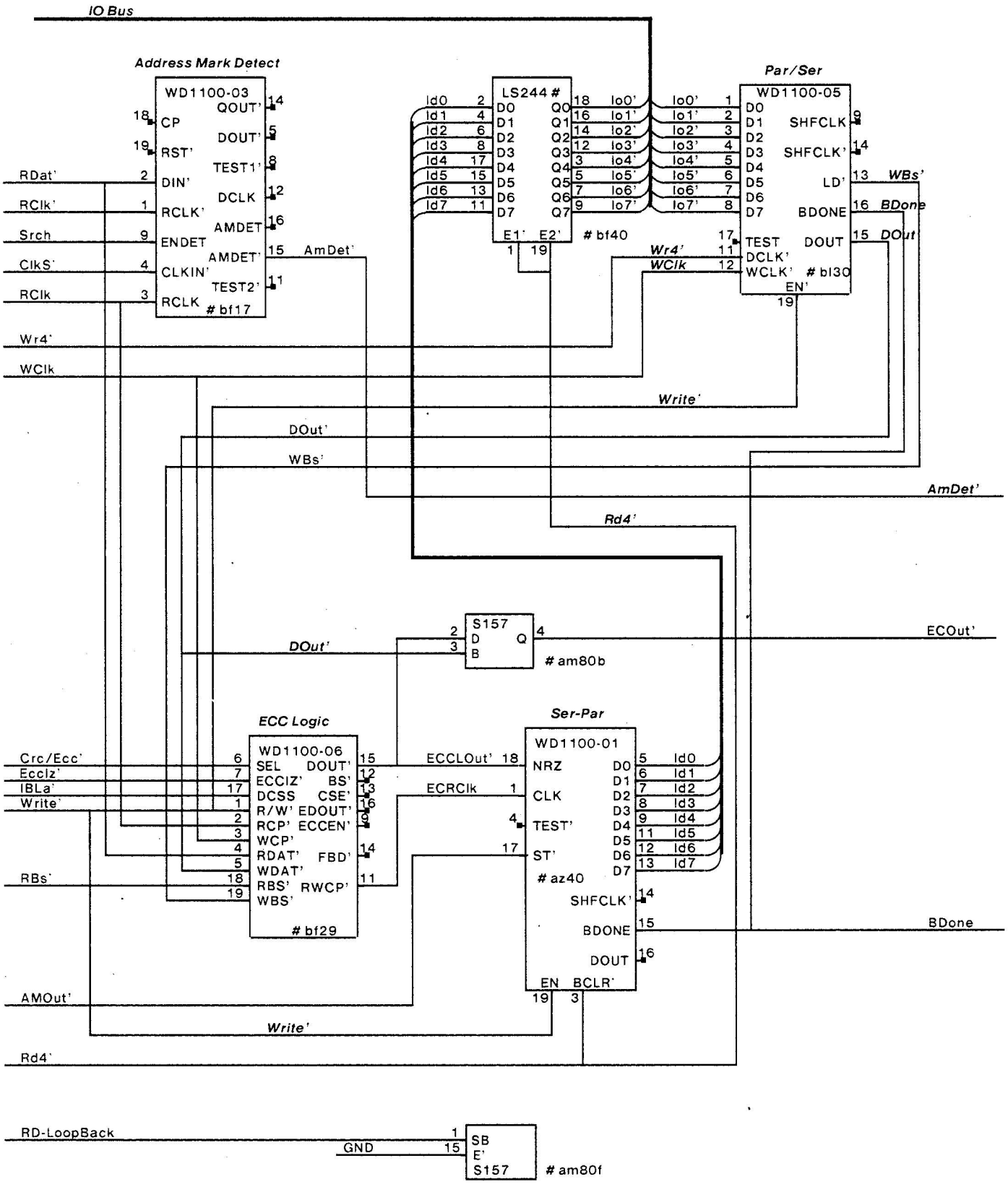
XEROX SDD	Project Dove	8x305 Data Store & I/O Decoding	File plOP29.sil	Designer Swenson	Rev A	Date 6/07/84	Page 29



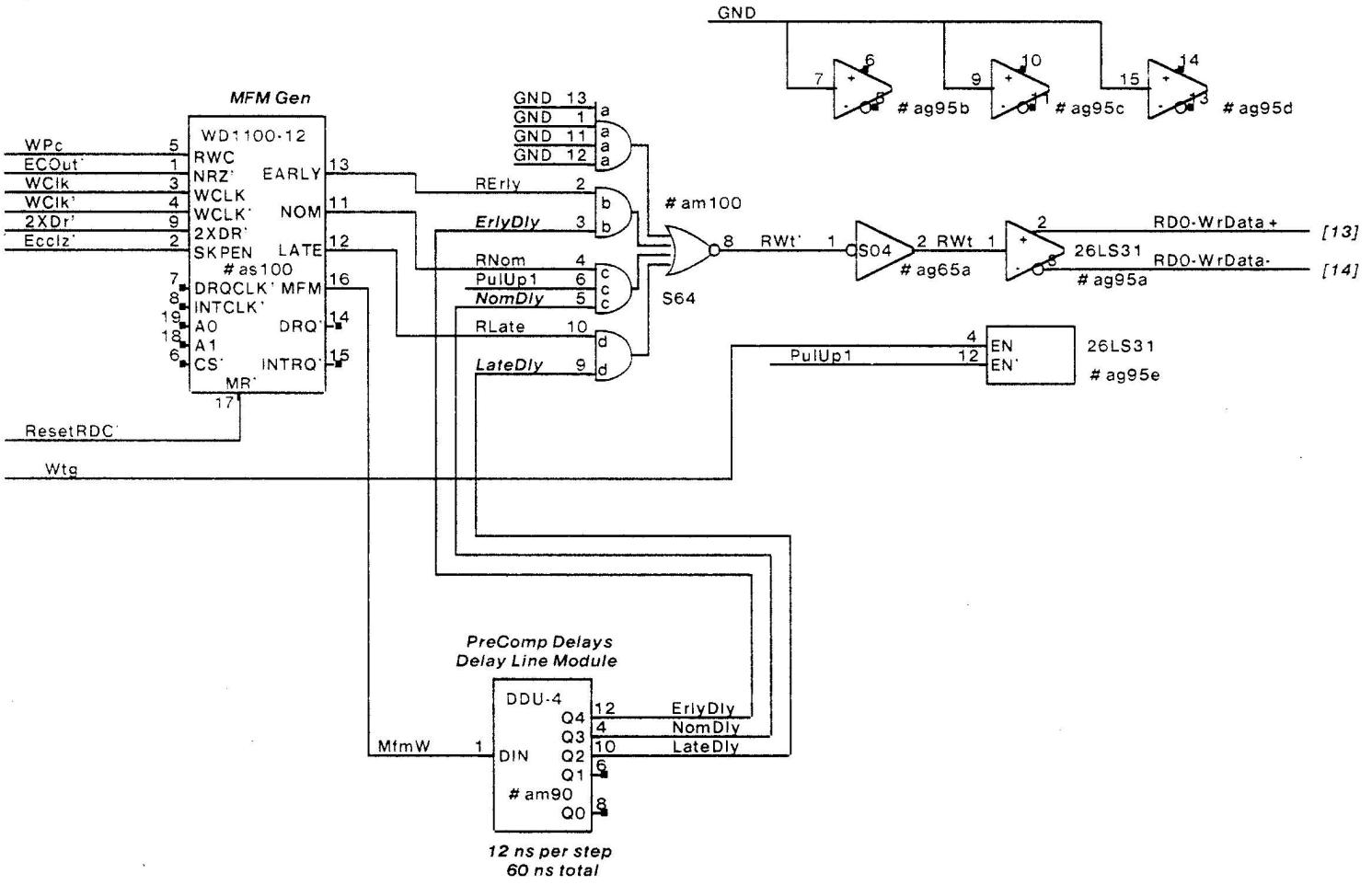
XEROX SDD	Project Dove	RDC Control Interface	File plOP30.sil	Designer Swenson, Oloumi	Rev A	Date 6/07/84	Page 30

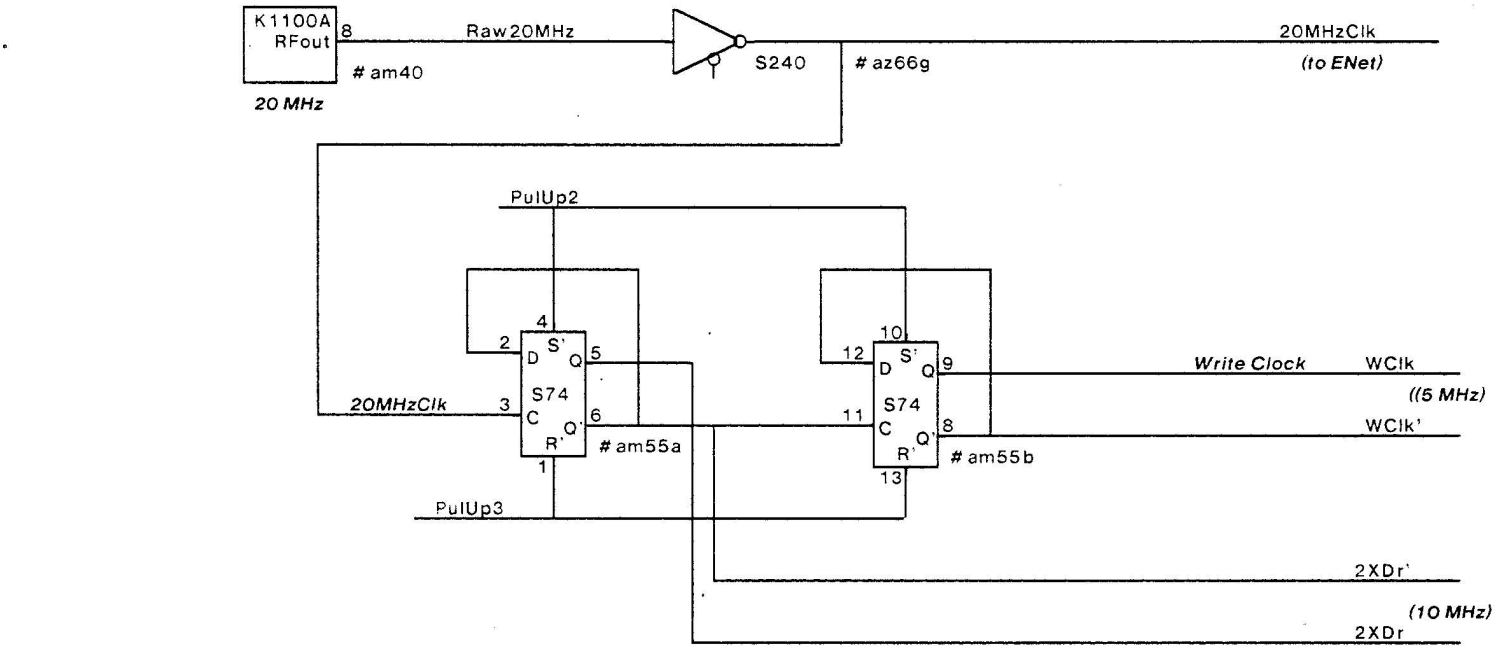


XEROX SDD	Project Dove	RDC Misc Interface	File pIOP31.sil	Designer Swenson	Rev A	Date 6/07/84	Page 31

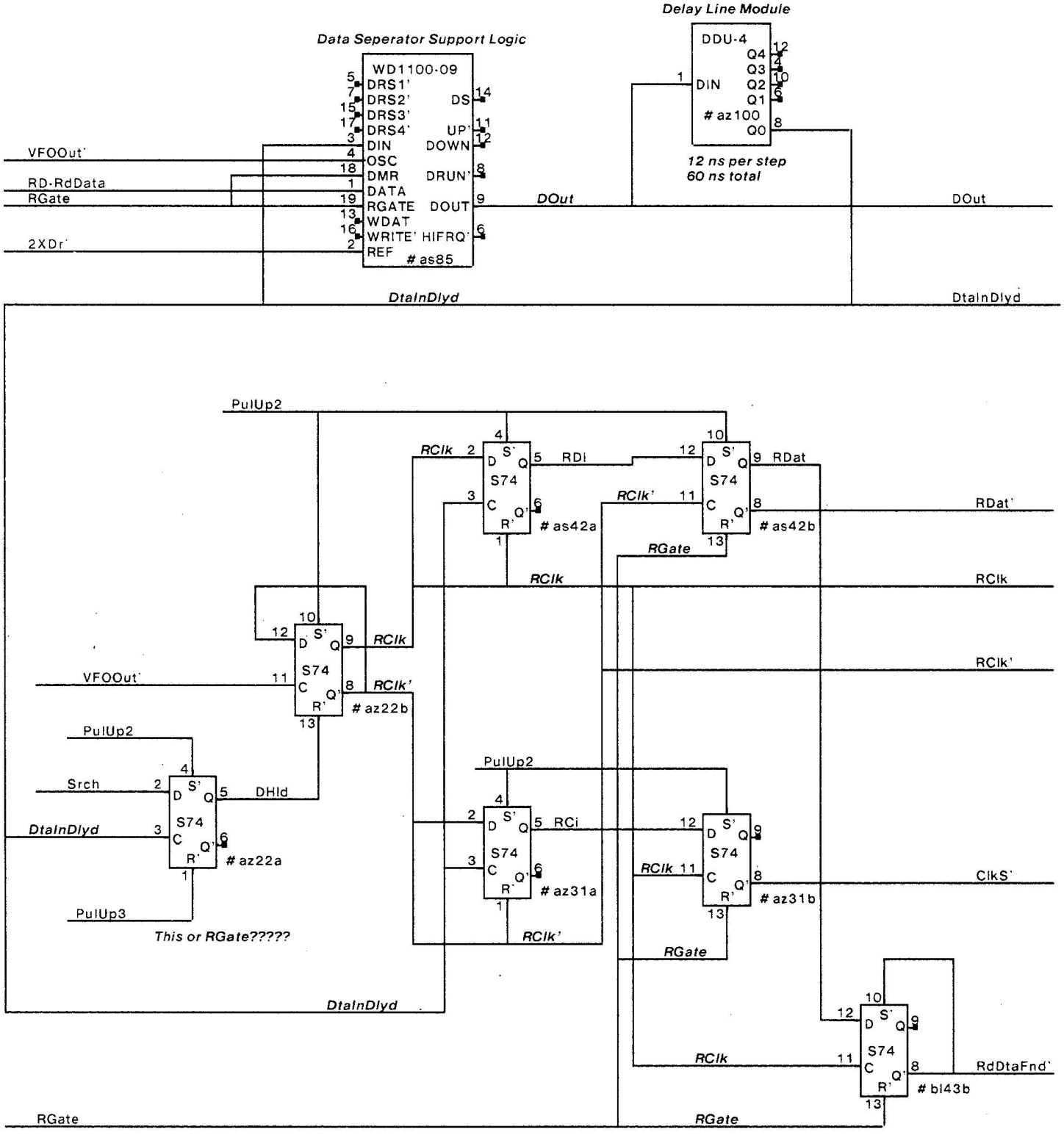


XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dove	RDC Serial Data Interface	plOP32.sil	Swenson	A	6/07/84	32

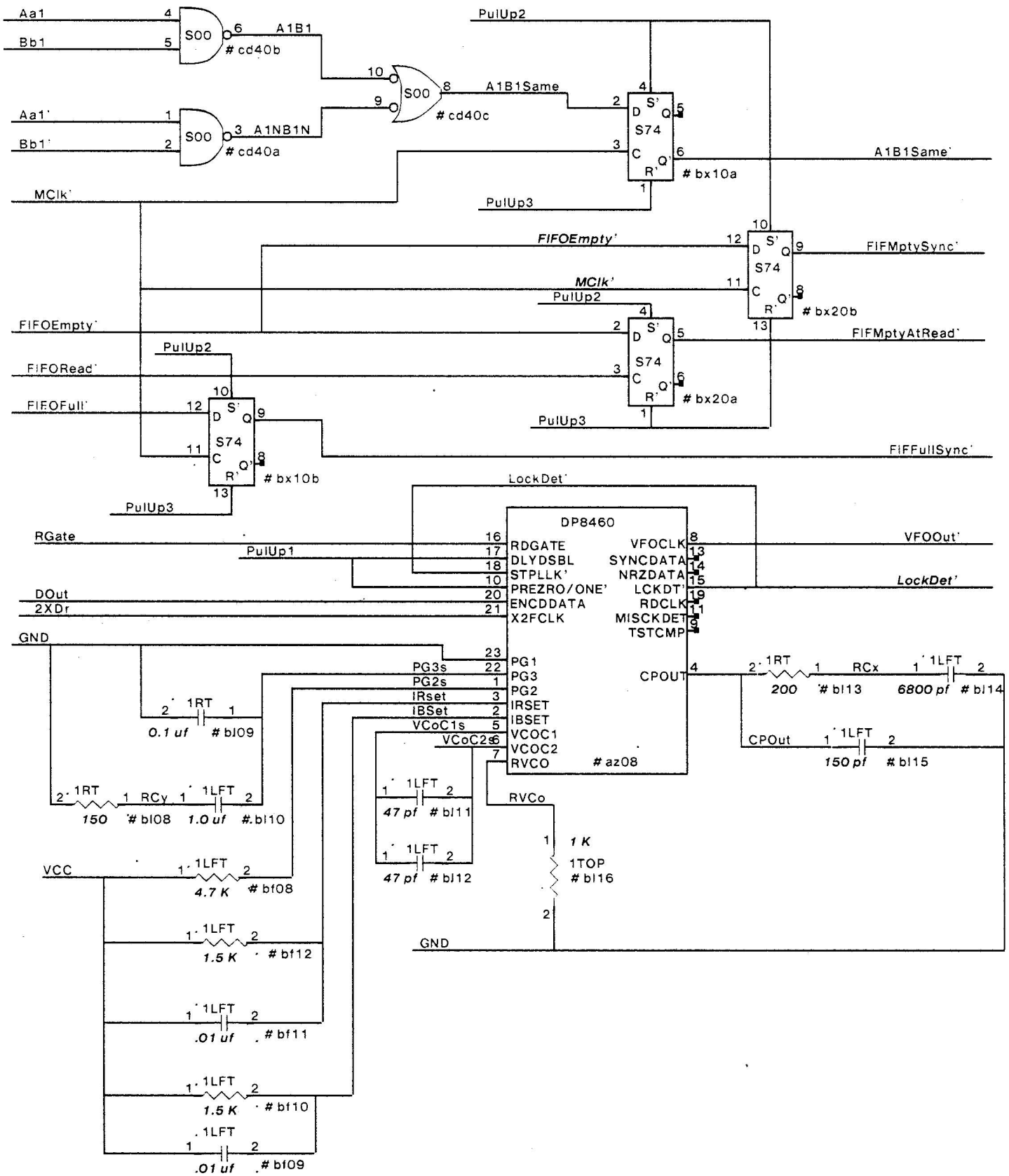




XEROX SDD	Project Dove	RDC Write Logic	File plOP33.sil	Designer Swenson	Rev A	Date 6/05/84	Page 33

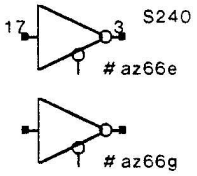


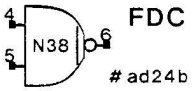
XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dove	RDC Data Separator	plOP34.sil	Swenson	A	6/07/84	34

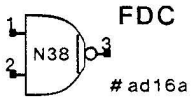


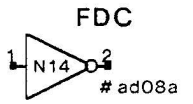
XEROX SDD	Project Dove	RDC PLL	File plOP35.sil	Designer Swenson, Oloumi	Rev A	Date 6/07/84	Page 35

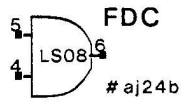
Spares

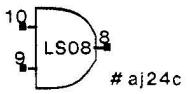


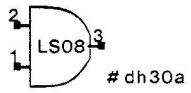


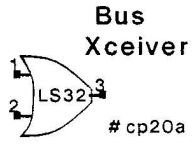


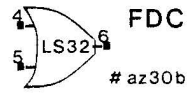


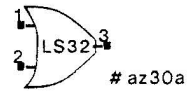




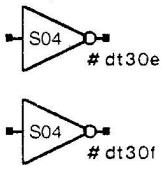


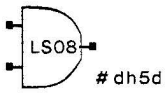


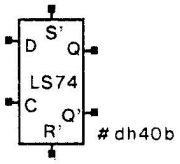




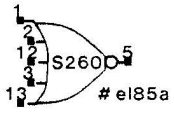
DMA

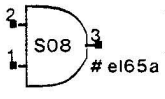


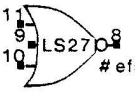




Arbitor







74393 - 1
Resistor - 0

XEROX SDD	Project Dove	Spares	File pIOP36.sil	Designer Tsang	Rev A	Date 6/07/84	Page 36

80186 IOP Related Signals :

AA.23	(tri,o)	J1.036
AA.22	(tri,o)	J1.039
AA.21	(tri,o)	J1.042
AA.20	(tri,o)	J1.045
AA.19	(tri,o)	J1.034
AA.18	(tri,o)	J1.037
AA.17	(tri,o)	J1.040
AA.16	(tri,o)	J1.043
AD.15	(bi)	J1.006
AD.14	(bi)	J1.009
AD.13	(bi)	J1.012
AD.12	(bi)	J1.015
AD.11	(bi)	J1.018
AD.10	(bi)	J1.021
AD.09	(bi)	J1.024
AD.08	(bi)	J1.027
AD.07	(bi)	J1.004
AD.06	(bi)	J1.007
AD.05	(bi)	J1.010
AD.04	(bi)	J1.013
AD.03	(bi)	J1.016
AD.02	(bi)	J1.019
AD.01	(bi)	J1.022
AD.00	(bi)	J1.025

S.2`	(tri,o)	J1.035
S.1`	(tri,o)	J1.038
S.0`	(tri,o)	J1.041
J1.017	AChipALE	
J1.056	AChipRd`	
J1.020	AChipWrH`	
J1.023	AChipWrL`	
J1.050	AChipLCS`	
186DT/R`	(tri,o)	J1.005
186DEn`	(tri,o)	J1.008
186BHE`	(tri,o)	J1.044
IOPUCS`		J1.049
IOPPCS.2`		J1.065
IOPPCS.3		J1.068
8MHzClk-bp		J1.029
16MHzClk-bp		J1.088
Reset-Sys`		J1.161
J1.014	MemRdy	
J1.073	DBrk/Daisy`	
J1.076	ParityCheck`	
J1.082	DpVertEvent`	
IOPI/ORd`		J1.048
IOPI/OWrH`		J1.054
IOPI/OWrL`		J1.057

IOP-MP Signals :

	CSWrEn	J1.095
	CSLoad/Shift`	J1.098
	CSBufferEn	J1.101
	CSDataIn	J1.104
	CSShiftClk	J1.107
J1.110	CSDataOut	
	HaltMesaP`	J1.103
	RstMesaP`	J1.109
	IOPIntrMesaP	J1.094
J1.097	MesaPIntrIOP	

IOP-Power Supply :

J1.160	PowerNormal	
J1.163	BootButton	
	LED1	J1.162
	LED2	J1.164
	LED3	J1.165

IOP-PCE Signals :

	IOPResetPC`	J1.066
	ArbHoldPCE	J1.072
J1.074	PCEHldaToArb	
J1.078	PCEIntrIOP`	

XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dove	165-pin System Connector - I	pIOP37.sil	Tsang	A	6/04/84	37

Rigid Disk Drive Signals :

For Drive 0 :

	RD0-DriveSeled'	*[1]*	*J1.111*
	RD0-WrData +	*[13]*	J1.108
	RD0-WrData-	*[14]*	J1.105
J1.102	RD0-RdData +	*[17]*	
J1.099	RD0-RdData-	*[18]*	

RD-ReduceWrtI'	*[2]*	J1.147
RD-WriteGate'	*[6]*	J1.144
RD-Step'	*[24]*	J1.135
RD-DirIn'	*[34]*	J1.130
RD-HeadSel0'	*[14]*	J1.139
RD-HeadSel1'	*[18]*	J1.138
RD-HeadSel2'	*[4]*	J1.145
RD-DriveSel0'	*[26]*	J1.133
RD-DriveSel1'	*[28]*	*J1.132*

J1.136	RD-Ready'	*[22]*
J1.137	RD-Index'	*[20]*
J1.142	RD-Track000'	*[10]*
J1.143	RD-SeekComp'	*[8]*
J1.141	RD-WriteFault'	*[12]*

Reserved for Drive 1 :

RD1-DriveSeled'	*[1]*	*J1.096*
RD1-WrData +	*[13]*	*J1.087*
RD1-WrData-	*[14]*	*J1.084*
RD1-RdData +	*[17]*	*J1.086*
RD1-RdData-	*[18]*	*J1.083*

Power :

VCC

J1.030	J1.115
J1.090	J1.116
J1.112	J1.117
J1.113	J1.119
J1.114	J1.120

GND

J1.026	J1.122
J1.028	J1.123
J1.031	J1.124
J1.032	J1.125
J1.033	J1.126
J1.061	J1.127
J1.062	J1.128
J1.063	J1.129
J1.069	J1.134
J1.085	J1.140
J1.089	J1.146
J1.091	J1.151
J1.092	J1.152
J1.093	J1.153
J1.121	J1.154
	J1.155
	J1.156

VEE *(-5V)*

J1.058
J1.059
J1.060

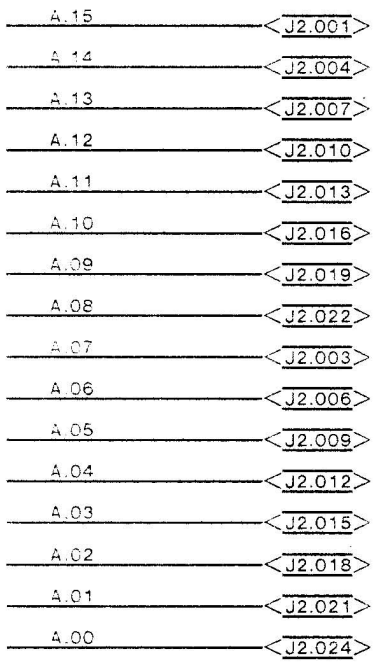
VDD *(+12V)*

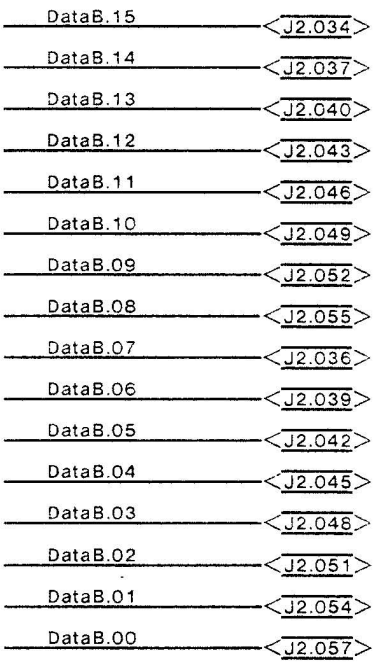
J1.157
J1.158
J1.159

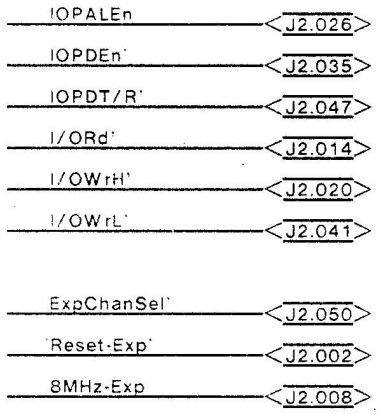
VBB *(-12V)*

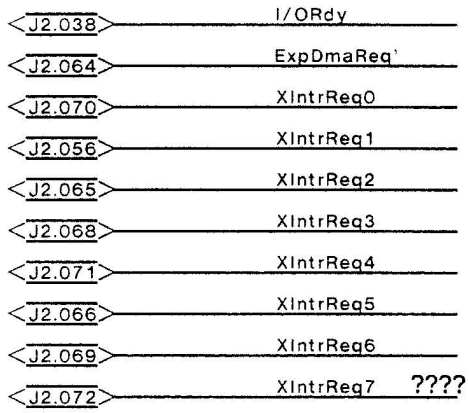
J1.148
J1.149
J1.150

XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dove	165-pin System Connector - II	pIOP38.sil	Tsang	A	6/06/84	38

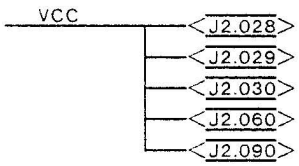


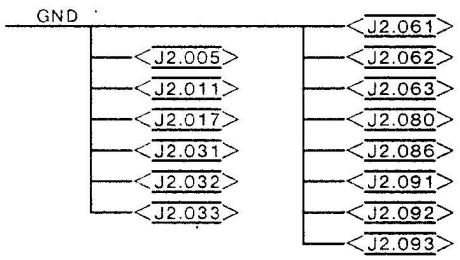


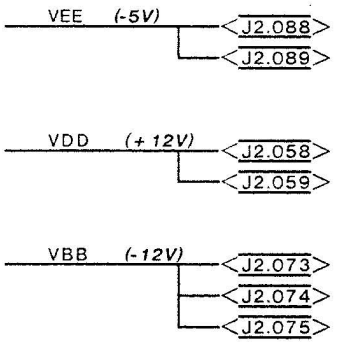




Power :







XEROX SDD	Project		File	Designer	Rev	Date	Page
	Dove	96-pin Expansion Connector	pIOP39.sil	Tsang	A	6/07/84	39